AuraVision

VxP202

Register Reference Manual

PRELIMINARY
DESIGN INFORMATION

Version 1.0

August 2, 1994

This data sheet contains preliminary data. AuraVision reserves the right to make changes without notice.
© Copyright 1994 AuraVision Corporation.

Table of Contents

Table of Contents 2
1.0 Registers Table 3
2.0 Register Description 6
PX Bus Configuration (6h) 6
... PX Bus Configuration (6h) Continued 7
I/O Base Address (10h) 8
Power On Reset Register (11h) 9
Memory Window Control (14h) 11
DRAM Control Register (17h) 12
Clock Frequency Low (27h) 13
Clock Frequency High (28h) 14
ISA Control (30h) 14
I2C Control (34h) 16
PLL Control A (36h) 17
PLL Control B (37h) 17
Input Configuration A (38h) 18
Input Configuration B (39h) 19
ISA Source Width A (3Ah) 21
ISA Source Width B (3Bh) 21
ISA Source Height A (3Ch) 21
ISA Source Height B (3Dh) 21
Horizontal Cropping Left A (40h) 22
Horizontal Cropping Left B (41h) 22
Horizontal Cropping Right A (44h) 22
Horizontal Cropping Right B (45h) 22
Vertical Cropping Top A (48h) 23
Vertical Cropping Top B (49h) 23
Vertical Cropping Bottom A (4Ch) 23
Vertical Cropping Bottom B (4Dh) 23
Filter Control (50h) 24
Horizontal Scaling Control A (54h) 25
Horizontal Scaling Control B (55h) 25
Vertical Scaling Control A (5Bh) 25
Vertical Scaling Control B (5Ch) 25
Picture Control Address (5Dh) 26
Picture Control Luma (5Eh) 26
Picture Control Chroma (5Fh) 26
Interrupt Control (60h) 27
Interrupt Status (61h) 28
Vin Multi-Buffer Depth A (68h) 29
Time Scaling Control (6Dh) 29
Video Layout Control (73h) 30
Input FIFO (78h) 30
Capture Control (80h) 31
Capture Viewport Width A (84h) 32
Capture Viewport Width B (85h) 32
Capture Viewport Height A (86h) 33
Capture Viewport Height B (87h) 33
Capture FIFO Thresholds (88h) 34
Capture Multi-Buffer Depth (8Ah) 35
Output FIFO Threshold Control (90h) 35
Out_req Active Level (91h) 35
Display Control (92h) 37
Multi-Buffer Depth Control (93h) 39
VGA Control (94h) 40
VGA Control B (95h) 42

Output Processing Control A (96h) 44
Output Processing Control B (97h) 45
Output Processing Control C (98h) 46
Palette Read Address (9Ah) 48
Chroma Key Control (9Bh) 48
Key Color (9Ch) 49
Key Color Hi (9Dh) 49
Key Color Hi 2 (9Eh) 49
Videon (Keyout) Control (9Fh) 49
View Port Starting Address A (A0h) 50
View Port Width A (A4h) 50
View Port Height A (A6h) 51
View Port Addr/Width/Height B (A7h) 51
View Port Display Origin Top A (A8h) 51
View Port Display Origin Left A (AAh) 51
View Port Display Origin Top/Left B (ABh) 52
Display Window Left A (B0h) 52
Display Window Right A (B4h) 52
Display Window Left/Right B (B5h) 52
Display Window Top A (B8h) 54
Display Window Bottom A (BCh) 54
Display Window Top/Bottom B (BDh) 54
Output Vertical Zoom Control A (C0h) 54
Output Vertical Zoom Control B (C1h) 55
Output Horizontal Zoom Control A (C4h) 55
Output Horizontal Zoom Control B (C5h) 56
Vertical Coordinate Offset (C6h) 56
Horizontal Coordinate Offset (C7h) 57
GPO Data 0 (CBh) 58
GPO Data 1 (CCh) 58
VGA Control C (CDh) 59
VGA Control D (CEh) 60
Max Hcount1 (D0h) 60
Max Hcount2 (D1h) 60
Interrupt Control (D2h) 62
Interrupt Status (D3h) 62
VGA Data Byte 0 (D5h) 64
VGA Data Byte 1 (D6h) 64
VGA Data Byte 2 (D7h) 64
Chroma Key Red Low (D8h) 64
Chroma Key Red High (D9h) 65
Chroma Key Green Low (DAh) 65
Chroma Key Green High (DBh) 65
Chroma Key Blue Low (DCh) 65
Chroma Key Blue High (DDh) 66
3.0 Register User's Guide 66
3.1 General Registers 66
3.2 Video-In Register 78
3.3 Video_Out Register 88
3.4 Capture Register 109

1.0 Registers Table

Index Register Address in Hexadecimal	Register Descrgisiption	Notes
06	PX Bus Configuration	
10	I/O Base Address	
11	Power On Reset	
14	Memory Window Control	
17	DRAM Control Register	
27	Clock Frequency Low	
28	Clock Frequency High	
30	ISA Control	
34	I2C Control	
36	PLL Control A	
37	PLL Control B	
38	Input Configuration A	
39	Input Configuration B	
3A	ISA Source Width A	
3B	ISA Source Width B	
3C	ISA Source Height A	
3D	ISA Source Height B	
40	Horizontal Cropping Left A	
41	Horizontal Cropping Left B	
44	Horizontal Cropping Right A	
45	Horizontal Cropping Right B	
48	Vertical Cropping Top A	
49	Vertical Cropping Top B	
4C	Vertical Cropping Bottom A	
4D	Vertical Cropping Bottom B	
50	Filter Control	
54	Horizontal Scaling Control A	
55	Horizontal Scaling Control B	
5B	Vertical Scaling Control A	
5C	Vertical Scaling Control B	
5D	Picture Control Address	
5E	Picture Control Luma	
5F	Picture Control	
60	Interrupt Control	
61	Interrupt Status	
68	Vin Multi-Buffer Depth A	
6D	Time Scaling Control	
73	Video Layout Control	
78	Input FIFO	
80	Capture Control	
84	Capture Viewport Width A	
85	Capture Viewport Width B	
86	Capture Viewport Height A	
87	Capture Viewport Height B	
88	Capture FIFO Thresholds	
8A	Capture Multi-buffer Depth	

90	Output FIFO Threshold Control	
91	Out_req Active Level	
92	Display Control	
93	Multi-buffer Depth Control	
94	VGA Control A	
95	VGA Control B	
96	Output Processing Control A	
97	Output Processing Control B	
98	Output Processing Control C	
9A	Palette Read Address	
9B	Chroma Key Control	
9C	Key Color	
9D	Key Color Hi	
9E	Key Color Hi 2	
9F	Videon (Keyout) Control	
A0	View Port Starting Address A	
A4	View Port Width A	
A6	View Port Height A	
A7	View Port Addr/Width/Height B	
A8	View Port Display Origin Top A	
AA	View Port Display Origin Left A	
AB	View Port Display Origin Top/Left B	
B0	Display Window Left A	
B4	Display Window Right A	
B5	Display Window Left/Right B	
B8	Display Window Top A	
BC	Display Window Bottom A	
BD	Display Window Top/Bottom B	
C0	Output Vertical Zoom Control A	
C1	Output Vertical Zoom Control B	
C4	Output Horizontal Zoom Control A	
C5	Output Horizontal Zoom Control B	
C6	Vertical Coordinate Offset	
C7	Horizontal Coordinate Offset	
CB	GPO Data 0	
CC	GPO Data 1	
CD	VGA Control C	
CE	VGA Control D	
D0	Max Hcount1	
D1	Max Hcount2	
D2	Interrupt Control	
D3	Interrupt Status	
D5	VGA Data Byte 0	
D6	VGA Data Byte 1	
D7	VGA Data Byte 2	
D8	Chroma Key Red Low	
D9	Chroma Key Red High	
DA	Chroma Key Green Low	
DB	Chroma Key Green High	
DC	Chroma Key Blue Low	
DD	Chroma Key Blue High	

2.0 Register Description

PX Bus Configuration (6h)

7	6	5	4	3	2	1	0
TO ENBLE	TOSEL 1	TOSEL 0	W/RN	MSTR1	MSTR0	SLV1	SLV0

Bit	Default	R/W	Description
1-0	00	R/W	Pipeline Slave Select 00 - Capture Pipeline is the Slave. 01 - Video Input Pipeline is the Slave. 10 - VIO (Hardware) Interface is the Slave. 11 - ISA Interface is the Slave.
3-2	00	R/W	Pipeline Master Select 00 - ISA Bus Interface is the Master. 01 - VIO Interface is the Master. 10 - Capture Pipeline is the Master. 11 - The Video Input Pipeline is Master.
4	0	R/W	Master Write/Read Select. 0 - The Master will Read from the Slave. 1 - The Master will Write to the Slave.
6-5	11	R/W	Timeout Duration Select. These bits select how long the ISA Bus Interface waits before it aborts an IOCHRDY cycle. When the cycle is aborted, the Timeout Interrupt Pending bit will be set in the ISA Control register (30h). 00 - 183 Memory Clock Cycles. 01 - 375 Memory Clock Cycles. 10 - 567 Memory Clock Cycles. 11 - 759 Memory Clock Cycles.
7	1	R/W	Timeout Enable. This bit enables a mode where long command cycles are aborted in order to comply with the ISA Bus minimum command active time of 15.18 microseconds. If this bit is set inactive low, an access to one of the pipelines could hold the ISA bus in an IOCHRDY state longer than 15.18 microseconds or indefinitly causing the system to hang. See The ISA Control register (30h) for details on the Timeout Interrupt. 0 - The Timeout Counter is Disabled.

... PX Bus Configuration (6h) Continued

Bit	Default	R/W	Description
4-0	00000	R/W	The following are legal combinations for bits 4 through 0 and how they configure the PX Bus for Interface/Pipeline transfer: val(hex) Transfer Type 00 - Software Capture. 04 - Hardware Capture with the VIO (Hardware) Interface as Master. 11 - Software Playback. 15 - Hardware Playback. 19 - Capture to Playback. -- Not operational 12 - Software to Hardware Playback. 02 - Hardware to Software Capture with ISA Interface as Master, reading from VIO Interface as Slave. 1A - Hardware Capture with Capture Pipeline as Master, writing to VIO as Slave. 1B - DMA Capture, with Capture Pipeline as Master, writing to ISA Interface as Slave. ISA Interface executes a DMA transfer using DREQ_V. 0F - DMA Playback, with Video Input Pipeline as Master, reading from ISA Interface as Slave. ISA Interface executes a DMA transfer using DREQ_V. Others - The Internal PX Bus is held inactive.

I/O Base Address (10h)

7	6	5	4	3	2	1	0
IOAD9	IOAD8	IOAD7	IOAD6	IOAD5	IOAD4	IOAD3	IOAD2

Bit	Default	R/W	Description
7-0	-	R/W	VxP202 I/O Base Address This register is initialized during reset from a bit pattern defined by pull-up and pull down resisters placed on the 8 LS bits of the SASD bus. The bit pattern defines a 4 byte region in the 10 bit ISA I/O space. Bits 15-11 of a correct ISA IO address must all be 0, bit 10 must be 1, bits 9 to 2 must match the I/O Base Address value, and bits 1 and 0 must match "00" for the index register, and "01" for the data register. This allows VxP501 to share I/O space with another 16 aware device. The first 16 bit word in the four byte region is the index port. The second word is the data port.

Power On Reset Register (11h)

7	6	5	4	3	2	1	0
		DSYNC EN	VIDN ACTH		565DIS		PRD

Bit	Default	R/W	Description
			Power On Reset value from the high byte of the SASD bus. This register is set during reset from a value defined by pull-up and pull down resisters placed on the 8 MS bits of the SASD bus.
0	-	R/W	Palette Read Disable. When 565 mode is enabled (see also POR10 below), this bit determines whether RAMDAC palette reads should be allowed. When 565 mode is disabled, RAMDAC palette reads are disabled regardless of the POR setting. Moreover, configuration register accessed (read or write accesses to 3C6 immideiately after 4 consecutive reads to 3C6) are always blocked. When the 565 mode is disabled, the external RAMDAC control signal RAMDACCMD is enabled and operates in the same way as the internal palette control signals.
2	-	R/W	565 Disable (POR10) This bit controls a set of register override functions. When this bit is set, the 565 (RAMDAC) mode is disabled. When this POR bit is cleared, the following VxP202 internal registers are overridden: vga_output_565_enable = 1 palette_ram_disable = 1 ramdac_cmd_enable = 1 Note that although ramdac_cmd is enabled, whether a read strobe is actually generated depends on the state of the palette read enable POR pin. Note also the the above registers are overridden but not changed. A read to those registers would return the contents of the registers. However, the VxP201 would operate not on the values in those register bits but on the values forced by the POR. In order to change any of the above settings, software must write to the above three bits then clear POR11 to remove the forced values.

3	-	R/W	Advanced Feature Connector Disable (POR11): When this bit is cleared the video outputs are tri-stated. This may be useful if the VxP201 is used in an Advanced Feature Connector application.
4	-	R/W	VIDEON Active High (POR12): When this bit is cleared, the VIDEON output goes low to indicate the video display region. When this bit is high, the VIDEON output goes high to indicate the video display region. On power up, the VIDEON output is set to following an internal register which defaults to 0 (not window and not color key).
5	-	R/W	Delayed Synce Enable (POR13): When this bit is set, the hsync and vsync output are delayed to match the internal pipeline delay of the rgb output (same as VxP500). When this bit is cleared, the hsync and vsync outputs follow the hsync and vsync inputs. This bit is should be cleared when an external bypass relay or bypass mux is used; otherwise, this bit should be set.

Memory Window Control (14h)

7	6	5	4	3	2	1	0
MWE	MWSZ	MWBA HIGH	MWBA 19	MWBA 18	MWBA 17	MWBA 16	MWBA 15

Bit	Default	R/W	Description
4-0	-	R/W	Memory window base address 19-15 These bits define the location in the chosen megabyte boundary (bit 5) of the VxP202 memory window. The granularity is in 32K or 128K blocks depending on bit 6.
5	0	R/W	Memory window base address 23-20 0 - "0000" first megabyte of ISA memory space. 1 - "1111" sixteenth megabyte of ISA memory space.
6	0	R/W	Memory window size 0 - 32K 1 - 128K
7	0	R/W	Memory window enable 0 - Disabled. No response to memory accesses. 1 - Enable. Respone to memory accesses to address in the range of the Memory Window Base Address to the MWBA + the Memory Window Size.

DRAM Control Register (17h)

7	6	5	4	3	2	1	0
TRSH 0		TRP 2	TRP 1	TRP 0	TRCD 1	TRCD 0	REF ENBL

Bit	Default	R/W	Description
0	1	R/W	Refresh Enable 0 - Refresh off. 1 - Refresh on.
2-1	1	R/W	tRCD (DRAM timing parameter). RAS active to CAS active delay. 0 - Two memory clock cycles. 1 - Three memory clock cycles. 2 - Four memory clock cycles 3 - Four memory clock cycles
5-3	3	R/W	tRP (DRAM timing parameter). RAS precharge time. 0 - Two memory clock cycle. 1 - Two memory clock cycles. 2 - Three memory clock cycles. 3 - Four memory clock cycles. 4 - Five memory clock cycles. others - RESERVED.
7	1	R/W	tRSH. (DRAM timing parameter) RAS hold time. 0 - Two memory clock cycles. 1 - Three memory clock cycles.

Clock Frequency Low (27h)

7	6	5	4	3	2	1	0
FREQ7	FREQ6	FREQ5	FREQ4	FREQ3	FREQ2	FREQ1	FREQ0

Bit	Default	R/W	Description
7-0	-	R	The frequency of the clock selected in register 28. The value is only valid when the index 28 register bit 7 is high and register bit 5 is low. Each read from this register restarts the counting sequence. The frequency can be measured to better than 1% accuracy for clocks that range from 10 to 90 MHz. The memory clock can be anywhere from 50 to 80 MHz. Frequency Formula: $f = 256 \cdot f_M / COUNT$ Where: f_M is the frequency of the memory clock $COUNT$ is the 10-bit counter value read from registers 27 and 28

Clock Frequency High (28h)

7	6	5	4	3	2	1	0
STBL	CLK SEL	CNTR RST			FREQ10	FREQ9	FREQ8

Bit	Default	R/W	Description
7	--	R	Frequency Stable. When high this bit indicates that the value currently currently stored in indexes 27 and 28 is a valid measure of the selected clock. If low the value is not yet stable. Whenever index 27 is read or bit 5 or 6 of this register toggle, the counting process will be restarted and this bit will go low. This bit will remain low until the final count has been reached and then go high. The same value will remain until then next read to 27 or toggle of bits 5 or 6.
6	0	R/W	Clock Select. When high, the Video Input clock is selected to be measured. When low, the video output clock is selected. When this bit changes the frequency counting process is restarted, the Frequency Stable bit (bit 7) will go low and when a valid count is reached bit 7 will go high.
5	1	R/W	Counter Reset. When high, both the frequency counter and the divider counter are held in a reset state in order to conserve power. When low, the divider counter will go active and the frequency counter will count up to the correct frequency. While the frequency counter is active bit 7 will be low. The divider counter will run continuously even after bit 7 goes high.
2-0	--	R	The three most significate bit of the frequency of the clock selected in register 28.

ISA Control (30h)

7	6	5	4	3	2	1	0
GLOB RST	TO INT MSK	ZWS CMD	ZWS EN	O128K	TDEC	MM	TO INT

Bit	Default	R/W	Description

0	0	R/W	ISA Timeout Interrupt Pending. This bit active high when an ISA interface timeout occurs. Timeouts occur when a Memory/IO Read/Write is issued from the CPU and the pipeline involved in the access can not respond within the programmed timeout interval (See the PX Bus Configuration Register -- 12h). If the timeout counter is disabled, no timeouts will occur. 0 - Reads: no timeout has occurred yet. Writes: clear the pending interrupt. 1 - Reads: a timeout has occurred. Writes: no effect.
1	0	R/W	Memory Mode. 0 - 8-bit wide DRAM data bus. 1 - 16-bit wide DRAM data bus.
2	0	R/W	Tight Decode Enable. 0 - The ISA bus signal MEMCS16 is not generated from a match of the combined LA/SA bus with the memory window base address. 1 - The ISA bus signal MEMCS16 is generated from a match of the combined LS/SA bus with the memory window base address. The ZEROWS signal cannot go active unless MEMCS16 is active early enough in the cycle.
3	0	R/W	Owner 128K decode enable. 0 - Owner 128K disabled. Use this setting when the memory window is mapped in a 128K memory block shared with another device. 1 - The ISA bus signal MEMCS16 is generated by decoding just the LA[23:17] address signals. The memory window must be mapped in a 128K area of memory that is not shared with another device (like a VGA card).
4	0	R/W	Zero Wait-State Enable. 0 - Disabled. The ZEROWS* signal will remain inactive. 1 - Enalbed. The ZEROWS* signal will go active for all 16-bit memory reads and writes. The MEMCS16* signal must go active in order for a Zero Wait-State cycle to occur.

5	1	R/W	ZEROWS* Command Mode. 0 - ZEROWS* timing is similar to MEMCS16* timing. It is a combinational decode of LA or LA/SA depending on the state of the Owner 128K Enable (bit 3) and Tight Decode Enable (bit 2). 1 - ZEROWS* timing follows the command. ZEROWS* is decoded based on TDEC and O128K above and is qualified with MEMR* or MEMW*. It is active only while the command is active.
6	0	R/W	ISA Timeout Mask. This bit acts as a mask for the ISA Timeout Pending bit (bit 0 of this register). 0 - No interrupt will occur when the ISA Timeout Pending bit goes active. 1 - An interrupt will occur when the ISA Timeout Pending bit goes active.
7	0	R/W	Global Reset 0 - Chip operates normally. 1 - Everything except I/O registers is held in a reset state. All registers may be read from or written to.

I2C Control (34h)

7	6	5	4	3	2	1	0
SFRS OUT	DATA CLKIN	DATA IN	CLK IN	DATA EN	DATA OUT	CLK EN	CLK OUT

Bit	Default	R/W	Description
0	0	R/W	I2C Clock Value 0 - low 1 - high
1	1	R/W	I2C Clock output enable 0 - Clock enabled 1 - Clock tri-stated with pull-up
2	0	R/W	I2C Data Value 0 - low 1 - high
3	1	R/W	I2C Data output enable 0 - Data enabled 1 - Data tri-stated with pull-up
4	-	R	I2C Clock read back value 0 - low 1 - high
5	-	R	I2C Data read back value 0 - low 1 - high
6	-	R	I2C Data read clock with external clock 0 - low 1 - high
7	-	W	Frame control output 0 - low 1 - high

These bits are reflected at the I2C pins immediately upon programming. The update bit in Input Configuration A has no effect on these bits. The global reset also has no effect on these bits.

PLL Control A (36h)

7	6	5	4	3	2	1	0
DIV 7	DIV 6	DIV 5	DIV 4	DIV 3	DIV 2	DIV 1	DIV 0

Bit	Default	R/W	Description
7-0	04	R/W	Divider low byte <7:0>

PLL Control B (37h)

7	6	5	4	3	2	1	0
PULSE 3	PULSE 2	PULSE 1	PULSE 0	DIV 11	DIV 10	DIV 9	DIV 8

Bit	Default	R/W	Description
3-0	D	R/W	Divider high byte <11:8>
7-4	0	T/W	Pulse width <3:0> When these bits are "0000" then the I2C_FRAME pin is sourced from the I2C register bit 7. Otherwise, the I2C_FRAME pin is sourced by the PLL clock divider.

The default value of divider is CF8h(=4096d-776d=3320d), The default value of pulse width is 2(count from 0 to 3), total number of clocks per line will be 780d.

Input Configuration A (38h)

7	6	5	4	3	2	1	0
TEST COMP	TEST RAM	DLY HSYNc	RST	VIDE	E SYNC	VSYC POL	HSYC POL

Bit	Default	R/W	Description
0	0	R/W	Horizontal sync polarity 0 - HSYNC is active low 1 - HSYNC is active high
1	0	R/W	Vertical sync polarity 0 - VSYNC is active low 1 - VSYNC is active high
2	0	R/W	Early syncs 0 - syncs have same timing as data 1 - syncs have same timing as tagn
3	0	R/W	Video Decoder/CL450 enable 0 - Diabled 1 - Enabled This bit turns on the video decoder input. Software reset does not have to be active to toggle this bit. When this bit is changed from 0 to 1, the input searches for a start of even field before activating the input decoder. Likewise when this bit is changed from 1 to 0, the input waits until the start of an even field before turning the input decoder off. This guarantees a clean data stream in the input pipeline.
4	0	R/W	Input pipeline reset 0 - No effect 1 - Reset input pipeline Write 1 to this bit to activate software reset for the input pipeline. Write 0 to clear software reset. This bit or the global reset will reset the input pipeline, but not the registers. This bit must be active while any input register is being programmed, except the VIDE bit in input configuration B.
5	0	R/W	horizontal sync delay 0 - No delay 1 - Delay one clock
7-6	0	R/W	Test mode for luma ram (256x8) and chroma ram (256x8) 01 - Test mode enable, test data is 55h. 11 - Test mode enable, test data is AAh

Input Configuration B (39h)

7	6	5	4	3	2	1	0
	VIO VIN_N	CNV SIGN	DIFF FMT	INTLC N	CPS EN	DAT FMT1	DAT FMT0

Bit	Default	R/W	Description
1-0	00	R/W	Input data format 00 - YUV 422 01 - RGB 15 (555) 10 - RGB 16 (565) 11 - Palettized These bits select the type of data at the either the decoder or the ISA input.
2	0	R/W	Enable Compressed buffer 0 - Disable Compressed buffer 1 - Enable Compressed buffer
3	0	R/W	Video scan type 0 - Interlace input 1 - Progressive input This bit selects whether the input is interlace or progrssive. If the input is interlace and this bit is set to progressive, then each field is treated as an independent frame. ISA playback is usually progressive, but in the case of HWPB the input may be interlace. The first field after reset is considered to be even.
4	0	R/W	Memory data type 0 - 6 bit 4:1:1 differential data 1 - 8 bit 4:2:2 dfferential data This bit selects the compressed data type of the memory.
5	0	R/W	Conver chroma sign enable 0 - Disable 1 - Enable This bit is used to convert between 2's complement and excess 128 notation for the chroma data. When this bit is set to 1, the polarity of the most significant bit of each chroma component is inverted.
6	0	R/W	VIO or VIN select 0 - Select VIN 1 - Select VIO

MEM_MODE	Input Type	Buffer Type	Configuration B
8 or 16 bit	YUV422	Comp422	XXX1X100
8 or 16 bit	YUV422	Comp411	XXX0X100

8 or 16 bit	YUV422	Uncompressed	XXXXX000
8 or 16 bit	RGB15	Comp422	XX01X101
8 or 16 bit	RGB15	Comp411	XX00X101
8 or 16 bit	RGB15	Uncompressed	XX0XX001
8 or 16 bit	RGB16	Comp422	XX01X110
8 or 16 bit	RGB16	Comp411	XX00X110
8 or 16 bit	RGB16	Uncompressed	XX0XX010
8 or 16 bit	Palettized	Comp422	XX01X111
8 or 16 bit	Palettized	Comp411	XX00X111
8 or 16 bit	Palettized	Uncompressed	XX00X011
8 bit	Comp422	Comp422	XX01X011
8 bit	Comp411	Comp411	XX01X011
16 bit	Comp422	Comp422	XX0XX000
16 bit	Comp411	Comp411	XX0XX000

ISA Source Width A (3Ah)

7	6	5	4	3	2	1	0
ISW 7	ISW 6	ISW 5	ISW 4	ISW 3	ISW 2	ISW 1	ISW 0

Bit	Default	R/W	Description
7-0	9Fh	R/W	ISA Source Width 7-0 This number should be set to 1 less than the actual width in 16 bit writes.

ISA Source Width B (3Bh)

7	6	5	4	3	2	1	0
						ISW 9	ISW 8

Bit	Default	R/W	Description
7-0	0	R/W	ISA Source Width 9-8

ISA Source Height A (3Ch)

7	6	5	4	3	2	1	0
ISH 7	ISH 6	ISH 5	ISH 4	ISH 3	ISH 2	ISH 1	ISH 0

Bit	Default	R/W	Description
7-0	77h	R/W	ISA Source Height 7-0 This number should be set to 1 less than the actual height in scan lines.

ISA Source Height B (3Dh)

7	6	5	4	3	2	1	0
						ISH 9	ISH 8

Bit	Default	R/W	Description
7-0	0	R/W	ISA Source Height 9-8

Horizontal Cropping Left A (40h)

7	6	5	4	3	2	1	0
HCL 7	HCL 6	HCL 5	HCL 4	HCL 3	HCL 2	HCL 1	HCL 0

Bit	Default	R/W	Description
7-0	0	R/W	Horizontal cropping Left 7-0

Horizontal Cropping Left B (41h)

7	6	5	4	3	2	1	0
						HCL 9	HCL 8

Bit	Default	R/W	Description
7-0	0	R/W	Horizontal cropping left 9-8

Horizontal Cropping Right A (44h)

7	6	5	4	3	2	1	0
HCR 7	HCR 6	HCR 5	HCR 4	HCR 3	HCR 2	HCR 1	HCR 0

Bit	Default	R/W	Description
7-0	ffh	R/W	Horizontal cropping right 7-0

Horizontal Cropping Right B (45h)

7	6	5	4	3	2	1	0
						HCR 9	HCR 8

Bit	Default	R/W	Description
7-0	03h	R/W	Horizontal cropping right 9-8

Vertical Cropping Top A (48h)

7	6	5	4	3	2	1	0
VCT 7	VCT 6	VCT 5	VCT 4	VCT 3	VCT 2	VCT 1	VCT 0

Bit	Default	R/W	Description
7-0	0	R/W	Vertical cropping top 7-0. This register should be set to an even value. This must be set to an even value in multi buffer modes.

Vertical Cropping Top B (49h)

7	6	5	4	3	2	1	0
						VCT 9	VCT 8

Bit	Default	R/W	Description
7-0	0	R/W	Vertical cropping top 9-8

Vertical Cropping Bottom A (4Ch)

7	6	5	4	3	2	1	0
VTB 7	VTB 6	VTB 5	VTB 4	VTB 3	VTB 2	VTB 1	VTB 0

Bit	Default	R/W	Description
7-0	ffh	R/W	Vertical cropping bottom 7-0

Vertical Cropping Bottom B (4Dh)

7	6	5	4	3	2	1	0
						VTB 9	VTB 8

Bit	Default	R/W	Description
7-0	03h	R/W	Vertical cropping bottom 9-8

Filter Control (50h)

7	6	5	4	3	2	1	0
VU_P	VD_O		VLF		HCF	HLF1	HLF0

Bit	Default	R/W	Description
1-0	0	R/W	Horizontal Luma Filter Mode 00 - No filtering 01 - 2 tap filtering (1 1)/2 10 - 3 tap filtering (1 2 1)/4 11 - 4 tap filtering (1 1 1 1)/4
2	0	R/W	Horizontal Chroma Filtering Control 0 - no filtering 1 - 2 tap filtering
4	0	R/W	Vertical Filtering Control 0 - no filtering 1 - 2 tap filter
6	0	R/W	Vertical Drop or Overwrite 0 - Drop 1 - Overwrite
7	0	R/W	Vertical Uniform or Paired 0 - Uniform 1 - Paired

Horizontal Scaling Control A (54h)

7	6	5	4	3	2	1	0
HSC 1	HSC 0						

Bit	Default	R/W	Description
7-6	0	R/W	Horizontal scaling contrl Set to 0 to diable scaling

Horizontal Scaling Control B (55h)

7	6	5	4	3	2	1	0
HSC 9	HSC 8	HSC 7	HSC 6	HSC 5	HSC 4	HSC 3	HSC 2

Bit	Default	R/W	Description
7-0	0	R/W	Horizontal scaling control

Vertical Scaling Control A (5Bh)

7	6	5	4	3	2	1	0
VSC 1	VSC 0						

Bit	Default	R/W	Description
7-6	0	R/W	Vertical scaling control Set to 0 to diable scaling.

Vertical Scaling Control B (5Ch)

7	6	5	4	3	2	1	0
VSC 9	VSC 8	VSC 7	VSC 6	VSC 5	VSC 4	VSC 3	VSC 2

Bit	Default	R/W	Description
7-0	0	R/W	Vertical scaling control

Picture Control Address (5Dh)

7	6	5	4	3	2	1	0
PCA 7	PCA 6	PCA 5	PCA 4	PCA 3	PCA 2	PCA 1	PCA 0

Bit	Default	R/W	Description
7-0	0	R/W	Picture control address The register content specify to addresses for the luma and chroma RAMs. Each RAM is 256X8.

Picture Control Luma (5Eh)

7	6	5	4	3	2	1	0
PCL 7	PCL 6	PCL 5	PCL 4	PCL 3	PCL 2	PCL 1	PCL 0

Bit	Default	R/W	Description
7-0	0	R/W	Picture control chroma data. Reading and writing to this register is essentially reading & writing data to the chroma ram.

Picture Control Chroma (5Fh)

7	6	5	4	3	2	1	0
PCC 7	PCC 6	PCC 5	PCC 4	PCC 3	PCC 2	PCC 1	PCC 0

Bit	Default	R/W	Description
7-0	0	R/W	Picture control luma data. Reading and writing to this register is essentially reading and writing data to the luma ram.

Interrupt Control (60h)

7	6	5	4	3	2	1	0
VIDE OFF	TC	FIFO DROP	CAP FIFO	VIDE ON	IN FRME	DEC ODD	DEC EVN

Bit	Default	R/W	Description
0	0	R/W	Interrupt source: input even field 0 - Disable 1 - Enable
1	0	R/W	Interrupt source: input odd field 0 - Disable 1 - Enable
2	0	R/W	Interrupt at the start of each frame which is captured. 0 - Disable 1 - Enable
3	0	R/W	Interrupt source: video enabled 0 - Disable 1 - Enable
4	0	R/W	Interrupt when capture FIFO contains data 0 - Disable 1 - Enable
5	0	R/W	FIFO data drop (overflow) 0 - Disable 1 - Enable
6	0	R/W	DMA TC 0 - Disable 1 - Enable
7	0	R/W	Interrupt source: video disabled 0 - Disable 1 - Enable

Interrupt Status (61h)

7	6	5	4	3	2	1	0
VIDE OFF	TC	FIFO DROP	CAP FIFO	VIDE ON	IN FRME	DEC ODD	DEC EVN

Bit	Default	R/W	Description
0	0	R/W	Interrupt source: input even field 0 - Disable 1 - Enable Set at the start of an even field from the video decoder. This bit needs to be cleared by software.
1	0	R/W	Interrupt source: input odd field 0 - Disable 1 - Enable Set at the start of an odd field from the video decoder. This bit needs to be cleared by software.
2	0	R/W	Interrupt at the start of each frame which is acquired. 0 - Disable 1 - Enable This bit is set when a frame is written to memory. Time scaled or dropped frames do not set this bit. This bit must be cleared by software.
3	0	R/W	Interrupt video decoder input enabled 0 - Cleared 1 - Enabled When the video decoder input goes active (start of even field) then this bit is set. This bit needs to be cleared by software.
4	0	R/W	Interrupt when capture FIFO contains data 0 - Disable 1 - Enable When the capture pipeline has the first piece of data from a frame to be read this bit goes active. This bit needs to be cleared by software.
5	0	R/W	FIFO data drop (overflow) 0 - Disable 1 - Enable When there is insufficient bandwidth to the memory controller this bit is set to show that input acquisition data has been dropped. This bit must be cleared by software.
6	0	R/W	DMA TC 0 - Disable 1 - Enable

7	0	R/W	Interrupt video decoder disabled 0 - Nothing 1 - Disabled When the video decoder input goes inactive (start of even field) then this bit is set. This bit needs to be cleared by software.

Vin Multi-Buffer Depth A (68h)

7	6	5	4	3	2	1	0
MBDP 7	MBDP 6	MBDP 5	MBDP 4	MBDP 3	MBDP 2	MBDP 1	MBDP 0

Bit	Default	R/W	Description
7-0	FF	R/W	Input Multi-Buffer Depth Marker. When the input reaches this line in the current frame, the buffer is freed so that one of the other sources can access it. This depth is relative to the line in memory. This register has 4 line granularity. Interlace mode is not supported because even or odd lines cannot be individually selected. Interlace can work in quad buffer if this depth is set to FFh.

Time Scaling Control (6Dh)

7	6	5	4	3	2	1	0
TC 7	TC 6	TC 5	TC 4	TC 3	TC 2	TC 1	TC 0

Bit	Default	R/W	Description
7-0	0	R/W	Time scaling factor When zero all fields are captured. Any other number represents the number of fields to capture for every 256 that enter. This feature operates on both the external decoder and the ISA data streams.

Video Layout Control (73h)

7	6	5	4	3	2	1	0
						VID LAYO 1	VID LAYO 0

Bit	Default	R/W	Description
1-0	0	R/W	Video Buffer Layout 0 - 512 vertical lines 1 - 256 vertical lines (8 bit memory) or 512 vertical lines (16 bit memory) with double buffering. 2 - 1024 vertical lines 3 - 256 vertical lines with quad buffering. These bits configure the available memory for a landscape, portrait, half size double buffer, or quarter size quadruple buffers. Because these bits change memory organization, they should only be changed during global reset.

Input FIFO (78h)

7	6	5	4	3	2	1	0
HI 3	HI 2	HI 1	HI 0	LO 3	LO 2	LO 1	LO 0

Bit	Default	R/W	Description
3-0	0	R/W	Input FIFO Low Marker When the FIFO depth becomes less than or equal to this value, the request becomes low priority.
7-4	0	R/W	Input FIFO High Marker. When the FIFO depth becomes greater than or equal to this value the request becomes high.

Capture Control (80h)

7	6	5	4	3	2	1	0
					1	CAP SFT RST	1

Bit	Default	R/W	Description
0	1	-	Reserved.
1	1	R/W	Capture Software Reset 0 - Capture Enabled 1 - Capture Disable (Capture Software Reset) This bit controls whether the capture pipeline is active or not. It is the software reset. Whwn active high, the Capture Pipeline will be held in reset but related register will not be effected. This bit must be 0 to program any registers pertainting to the capture pipeline since the registers are not synchronized to the capture pipeline.
2	1	-	Reserved.

Capture Viewport Width A (84h)

7	6	5	4	3	2	1	0
CPWD 7	CPWD 6	CPWD 5	CPWD 4	CPWD 3	CPWD 2	CPWD 1	CPWD 0

Bit	Default	R/W	Description
7-0	4fh	R/W	Capture Viewport Width in memory accesses. This register should be set to one less than the number of memory accesses. A memory access is either 8 or 16 bits depending on memory mode.

Capture Viewport Width B (85h)

7	6	5	4	3	2	1	0
							CPWD 8

Bit	Default	R/W	Description
7-0	0	R/W	Capture Viewport Width

Capture Viewport Height A (86h)

7	6	5	4	3	2	1	0
CPHD 7	CPHD 6	CPHD 5	CPHD 4	CPHD 3	CPHD 2	CPHD 1	CPHD 0

Bit	Default	R/W	Descriptio
7-0	77h	R/W	Capture Viewport Height in scan lines. The height is one less than the number of lines.

Capture Viewport Height B (87h)

7	6	5	4	3	2	1	0
						CPHD 9	CPHD 8

Bit	Default	R/W	Description
7-0	0	R/W	Capture Viewport Height.

Capture FIFO Thresholds (88h)

7	6	5	4	3	2	1	0
HI 3	HI 2	HI 1	HI 0	LO 3	LO 2	LO 1	LO 0

Bit	Default	R/W	Description
3-0	4	R/W	Capture FIFO Low Marker Whwn the FIFO depth becomes less than or equal to this value, the request becomes high priority. The msb of the depth is ’0’ for the new marker.
7-4	8	R/W	Capture FIFO High Marker. When the FIFO depth becomes greater than or equal to this value the request becomes low. The msb of the depth is ’1’ for the high marker.

Capture Multi-Buffer Depth (8Ah)

7	6	5	4	3	2	1	0
MBDP 7	MBDP 6	MBDP 5	MBDP 4	MBDP 3	MBDP 2	MBDP 1	MBDP 0

Bit	Default	R/W	Description
7-0	ffh	R/W	Capture Multi-Buffer depth Marker When the capture reaches this line in the current frame, the buffer is freed so that one of the other sources can access it. If this marker is not reached then the marker is cleared before the next buffer is entered. The marker has a granularity of 4 lines.

Output FIFO Threshold Control (90h)

7	6	5	4	3	2	1	0
OFHO 3	OFHO 2	OFHO 1	OFHO 0	OFLO 3	OFLO 2	OFLO 1	OFLO 0

Bit	Default	R/W	Description
3-0	1100	R/W	Output FIFO low threshold These bits set the level at which the output FIFO makes a preemptive memory request. The actual fifo depth is 2 above this value. The most significant bit of the depth is set to '0' for the low threshold.
7-4	1000	R/W	Output FIFO high threshold These bits set the level at which the output FIFO makes a preemptive memory request. The actual fifo depth is 2 above this value. The most significant bit of the depth is set to '1' for the high threshold.

Out_req Active Level (91h)

7	6	5	4	3	2	1	0
			ORL 4	ORL 3	ORL 2	ORL 1	ORL 0

Bit	Default	R/W	Description
4-0	10110	R/W	Out_req active level These bits set the transistion value of fifo_write_depth. If fifo depth is less-than-or-equal to this register value, out_req goes high, else it is low

Display Control (92h)

7	6	5	4	3	2	1	0
VID_DW	VGA_CH_K	VID_COL_K	VORS1	VORS0	VDWE	V1KE	VCKE

Bit	Default	R/W	Description
0	0	R/W	VGA color key enable 0 - Disable 1 - Enable When disabled, a color key match is generated regardless of the color key specification.
1	0	R/W	VGA 1555 key enable 0 - Disable 1 - Enable In the case where a 16 bit direct color VGA is used with the VxP202 and the VGA controller is in 555 TARGA format with an embedded key in the most significant bit, enabling this bit allows the embedded key to act as the VGA color key. (Enable bit 0 also when enabling this bit). This bit must be set to zero when not in 555 mode.
2	0	R/W	VGA display window enable 0 - Disable 1 - Enable When disabled, a display window match is generated regardless of the display window specification.
4-3	11	R/W	Video output region select. 00 - Key and display window. 01 - Display window but not key. 10 - Key but not display window. 11 - Not key and not display window.
5	1	R/W	Video in color key region (high speed bypass mode only) 0 - Video in non-color key region 1 - Video in color key region This bit controls the function of VIDEON only when High speed data path is (bit 4 of VGA Control B) is enabled. When set to 1, VIDEON is active in the color key region of the display. When set to 0, VIDEON is active in the non-color key region of the display. If VGA color key (bit 0) is disabled then the color key region will cover the entire display region.

6	1	R/W	VGA in chroma key region (high speed bypass mode only) 0 - VGA in non-chroma key region 1 - VGA in chroma key region This bit controls the function of VIDEON only when High speed data path is (bit 4 of VGA Control B) is enabled. When set to 1, VIDEON is inactive (dispaly VGA) in the chroma key region of the display. When set to 0, VIDEON is inactive in the non-chroma key region of the display. If chroma key (bit 6 of Output Processing Control A) is disabled then the chroma key region will not exist.
7	1	R/W	Video in display window region (high speed bypass mode only) 0 - Video in non-display window region 1 - Video in display window region This bit controls the function of VIDEON only when High speed data path is (bit 4 of VGA Control B) is enabled. When set to 1, VIDEON is active in the dispaly window region of the display. When set to 0, VIDEON is active in the non-display window region of the display. If VGA display window (bit 0) is disabled then the display window region will cover the entire display region.

Multi-Buffer Depth Control (93h)

7	6	5	4	3	2	1	0
MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0

Bit	Default	R/W	Description
7-0	3CH	R/W	Multi-buffer depth control This register specifies the line at which the buffer being display may be released. The line number is the value in this register multiplied by 2. This register must be setup before enabling multi-buffer modes.

VGA Control (94h)

7	6	5	4	3	2	1	0
VGAF	DCM1	DCM0	DCDC	DC16E	HSP	VSP	INLC

Bit	Default	R/W	Description
0	0	R/W	VGA display mode 0 - Non-interlaced 1 - Interlaced
1	0	R/W	VGA vertical sync polarity 0 - Active low 1 - Active high
2	0	R/W	VGA horizontal sync polarity 0 - Active low 1 - Active high
3	0	R/W	VGA direct color 16 enable, change on falling edge of write. 0 - Disable 1 - Enable
4	0	R/W	VGA direct color double clock, change on falling edge of write. 0 - Disable 1 - Enable
6-5	00	R/W	16 bit direct color mode 00 - RGB: 555 01 - RGB: 565 10 - RGB: 664 11 - RGB: 655

7	0	R/W	VGA field 0 - field 1 1 - field 0 At the leading edge of VGA vsyncs, the VxP202 checks if interlaced mode is turned on. If so, it sets the internal VGA field indicator to the value of this bit. The internal field indicator is toggle on evey VGA vsync until interlaced mode is turned off. Software should write the first VGA pixels of the first two VGA lines with different value, wait for a vsync and blank high then read the VGA data. If the data read is what was written on the first line, the current VGA field is 0. Software should write 0 into the VGA field bit to indicate that the next field will be 1. Similarly, if the data read is what was written on the second line, the current VGA field is 1 and the VGA field bit should be set to 1.

VGA Control B (95h)

7	6	5	4	3	2	1	0
AFCE	AFC EME	HSCK EN	HSCS 1	HSCS 0	EVEN STATE	EVEN INC	DC24

Bit	Default	R/W	Description
0	0	R/W	24 bit direct color VGA enable 0 - VGA data is not 24 bit direct color 1 - VGA data is 24 bit direct color Enables 24 bit bit direct color mode. VGA clock is assumed to be three times the pixel clock and data are in 888 format. This bit and the 16 bit direct color enable bit should not be set together. When both bits are cleared, the VGA is in 8 bit palettized mode.
1	0	R/W	Even field vcount initial value 0 - VGA internal line counting begins with 1 1 - VGA internal line counting begins with 3 The even field count can start on a wrong value due to offset hsync and vsync. Software can test for the two cases and set this bit appropriately when in interlaced mode to assure correct line counting values
2	0	R	Even field state value, read only For software to have enough information to set bit 1 above correctly, it will need to know whether the hardware is counting the first even field line or not. This bit will be 0 if it is not counting it.
4-3	10	R/W	High speed video clock select 0 - VGA clock 1 - 1/2 VGA clock 2 - 1/3 VGA clock 3 - 1/4 VGA clock When the clock is switched, the clock may stop until the next blank signal. During that time, the registers may not be functional. Software should wait for the next blank before writing to registers again. Also, software should disable the videoout pipeline (bit 5 of OUT_PROC_CTL_B) when changing the clock select value to ensure that a temporarily stopped video clock signal will not create a lock-up scenerio.

5	0	R/W	High speed data path enable 0 - Disabled 1 - Enabled When set, this bit enables the high speed vga data path. In this case, the RGB output is from the hzoom block, the key output is from the high speed compare, and the video clock is from the high speed clock generator.
6	0	R/W	Advanced feature connector extended mode enabled 0 - baseline mode 1 - extended mode In baseline mode, data are output after horizontal zoom. Display window and color keying should be turned off. Position of the display window is controlled by the viewport display origin. In extended mode, data are output before horizontal zoom. The viewport size must be identical to the graphic controller video window size.
7	0	R/W	Advanced feature connector enable 0 - Disable 1 - Enable When enabled, the following pins are mapped to advanced feature connector functions. vga_clock_out: afc_clock_out vga_red_out(5): gpo(9) vga_red_out(4): gpo(8) vga_red_out(3:0): afc_red_out(4:1) vga_green_out(5): afc_red_out(0) vga_green_out(4:0): afc_green_out(5:1) vga_blue_out(5): afc_green_out(0) vga_blue_out(4:0): afc_blue_out(4:0) videon: afc_vrdy_out vga_data(0): afc_grdy_in vga_data(1): afc_fstat_in

Output Processing Control A (96h)

7	6	5	4	3	2	1	0
	CKE	CIE			HIE	HZME	

Bit	Default	R/W	Description
1	0	R/W	Horizontal zoom enable 0 - Disable 1 - Enable
2	0	R/W	Horizontal interpolation enable 0 - Disable 1 - Enable
5	0	R/W	Chroma interpolation enable 0 - Disable 1 - Enable When enabled, 4:1:1 or 4:2:2 YUV data are linearly interpolated into 4:4:4 YUV data.
6	0	R/W	Chroma key enable 0 - Disable 1 - Enable

Output Processing Control B (97h)

7	6	5	4	3	2	1	0
RLE	VRST	VEN				VIE	VZME

Bit	Default	R/W	Description
0	0	R/W	Vertical zoom enable 0 - Disable 1 - Enable
1	1	R/W	Vertical zoom interpolate enable 0 - Disable 1 - Enable
4-2			Reserved
5	1	R/W	Video output enable 0 - Disable 1 - Enable
6	0	R/W	Video output reset 0 - Disable 1 - Enable
7	0	R/W	Viewport control registers load enable 0 - Disable 1 - Enable When this bit is set, the viewport control register values are transferred into the video output processing blocks at the beginning of the next viewport. When this bit is cleared, control register values are not tranferred into the processing blocks. This bit is cleared on reset. After initial viewport control register programming, this bit should be set to enable transfer into the processing blocks. To reprogram the viewport control registers, this bit should first be cleared to prevent partially programmed viewport definitions to be transferred into the processing blocks. When all necessary viewport control registers are programmed, this bit should be set to enable the transfer.

Output Processing Control C (98h)

7	6	5	4	3	2	1	0
HZ2	ADLY EN	SDLY EN	MUX MODE	MUX EN		IMUX EN	565 EN

Bit	Default	R/W	Description
0	0	R/W	565 output enable 0 - Disable 1 - Enable Normally the output is either 18 bits direct output or 8 bits multiplexed output. When this bit is enabled (mux mode should be disabled), 16 bits of 565 data are output on red(3:0), green(5:0) and blue(5:0). Red(5:4) become general purpose output pins. If RAMDAC control is also enabled, red(5:4) become RAMDAC control pins. NOTE : 565 always enabled when por(10) = '0'
1	1	R/W	Internal muxing enable 0 - Disable 1 - Enable When this bit is cleared, the VxP202 internal digital mux is disabled. This bit should be cleared when external analog muxing is used.
3	0	R/W	VGA output data mux enable 0 - Disabled 1 - Enabled When the vga output mux is disabled, the RGB data are output on the 18 bit RGB outputs (same as VxP500). When enabled, the RGB data are converted from 18 bits into 16 bits 565 format and output on the G[1:0] and B[5:0] pins. The remaining 10 pins become general purpose output pines and take on the values in the GPO registers. When the VGA is in 1X clock mode, data are output using the raising and falling edge of the vga output clock. When the VGA is in 2X or 3X clock mode, data may be output using the 2X or 3X clock.
4	0	R/W	VGA output data mux mode 0 - Mux data out on rising and falling edge 1 - Mux data out on rising edge only When the VGA is in 2X or 3X clock mode, data may be output using the 2X or 3X clock.

5	1	R/W	DAC clock invert enable 0 - Disabled 1 - Enabled This bit should be set when in the VGA is in palettized mode. This bit inverts the DAC clock and ensures proper setup and hold time for the DAC. This bit should be cleared when the VGA is in 16 bit color mode.
6	0	R/W	DAC output delay enable 0 - Disabled 1 - Enabled This bit delays the DAC clock by approximately 3 ns.
7	0	R/W	Horizontal zoom by 2 0 - Disabled 1 - Enabled The output data is zoomed horizontally by 2. This mode is intented for high speed VGA modes (1024x768 NI) where the video data is zoomed horizontally by 2 to keep the video pipeline operating under 45MHz. When this bit is set, the video clock is half the vga clock speed. The pixel mask of the internal palette should be set to 0 to reduce current consumption.

Palette Read Address (9Ah)

7	6	5	4	3	2	1	0
		PHSD		PAHN 3	PAHN 2	PAHN 1	PAHN 0

Bit	Default	R/W	Description
3-0	0010	R/W	Palette address high nibble These bits specify the lower nibble of the palette adddress
5	0	R/W	Palette hidden register snoop disable 1 - Disabled 0 - Enabled

Chroma Key Control (9Bh)

7	6	5	4	3	2	1	0
					CKD 2	CKD 1	CKD 0

Bit	Default	R/W	Description
2-0	000	R/W	Chroma key delay for high speed bypass

Key Color (9Ch)

7	6	5	4	3	2	1	0
KC 7	KC 6	KC 5	KC 4	KC 3	KC 2	KC 1	KC 0

Bit	Default	R/W	Description
7-0	254	R/W	VGA key color value 7-0 These bits specify the color key for 8 palettized VGA data or the byte 0 of the color key for 16 bit direct color VGA data.

Key Color Hi (9Dh)

7	6	5	4	3	2	1	0
KC 15	KC 14	KC 13	KC 12	KC 11	KC 10	KC 9	KC 8

Bit	Default	R/W	Description
7-0	254	R/W	VGA key color value 15-8 These bits specify byte 1 of the color key for 16 bit direct color VGA data.

Key Color Hi 2 (9Eh)

7	6	5	4	3	2	1	0
KC 23	KC 22	KC 21	KC 20	KC 19	KC 18	KC 17	KC 16

Bit	Default	R/W	Description
7-0	254	R/W	VGA key color value 23-9 These bits specify byte 2 of the color key for 24 bit direct color VGA data.

Videon (Keyout) Control (9Fh)

7	6	5	4	3	2	1	0
		VIDND 2	VIDND 1	VIDND 0		VIDN OVST	VIDN EN

Bit	Default	R/W	Description

0	0	R/W	Videon (analog mux key) enable 0 - Disable 1 - Enable
1	0	R/W	Videon overwrite state 0 - VIDEON = low 1 - VIDEON = high Videon (analog mux key) is overwritten to this state when bit 0 of this register is disabled and bits 5:3 are set to 2 (4 clocks) or larger. This data is inverted when the power on reset for key out, por(12), is set to active low.
5-3	0	R/W	Videon out delay and high speed bypass color key delay. These bits should not be set to zero when in 16 bit/pixel or 24 bit/pixel mode. 0 - 2 clocks 1 - 3 clocks ... 7 - 9 clocks

View Port Starting Address A (A0h)

7	6	5	4	3	2	1	0
VPA 7	VPA 6	VPA 5	VPA 4	VPA 3	VPA 2	VPA 1	VPA 0

Bit	Default	R/W	Description
7-0	0	R/W	View port address These registers specify the memory line in the frame buffer containing the upper edge of the view port.

View Port Width A (A4h)

7	6	5	4	3	2	1	0
VPW 7	VPW 6	VPW 5	VPW 4	VPW 3	VPW 2	VPW 1	VPW 0

Bit	Default	R/W	Description
7-0	6BH	R/W	View port width in frame buffer memory words. The number of frame buffer words is one plus the number specified in these bits. That is, a register value of 0 specifies a view port width of 1 word and a register value of 1FF specifies a view port width of 512 words. The minimum width, however, is 2 words.

View Port Height A (A6h)

7	6	5	4	3	2	1	0
VPH 7	VPH 6	VPH 5	VPH 4	VPH 3	VPH 2	VPH 1	VPH 0

Bit	Default	R/W	Description
7-0	F0h	R/W	View port height in lines The number of frame buffer lines is one plus the number specified in these bits. That is, a register value of 0 specifies a view port height of 1 line and a register value of 3FF specifies a view port height of 1024 lines.

View Port Addr/Width/Height B (A7h)

7	6	5	4	3	2	1	0
VPA 9	VPA 8		VPW 8			VPH 9	VPH 8

Bit	Default	R/W	Description
1-0	0	R.W	View port height in frame buffer lines
4	0	R/W	View port width in frame buffer memory words
7-6	0	R/W	View port address

View Port Display Origin Top A (A8h)

7	6	5	4	3	2	1	0
VPTO 7	VPTO 6	VPTO 5	VPTO 4	VPTO 3	VPTO 2	VPTO 1	VPTO 0

Bit	Default	R/W	Description
7-0	100	R/W	View port display origin top in VGA lines from VGA VSYNC.

View Port Display Origin Left A (AAh)

7	6	5	4	3	2	1	0
VPLO 7	VPLO 6	VPLO 5	VPLO 4	VPLO 3	VPLO 2	VPLO 1	VPLO 0

Bit	Default	R/W	Description
7-0	100	R/W	View port display origin in VGA pixel clock from VGA HSYNC

View Port Display Origin Top/Left B (ABh)

7	6	5	4	3	2	1	0
VPTO 9	VPTO 8				VPLO 10	VPLO 9	VPLO 8

Bit	Default	R/W	Description
2-0	0	R/W	View port display origin left in VGA pixel clock from VGA HSYNC
7-6	0	R/W	View port display origin top in VGA lines from VGA VSYNC

Display Window Left A (B0h)

7	6	5	4	3	2	1	0
DWL 7	DWL 6	DWL 5	DWL 4	DWL 3	DWL 2	DWL 1	DWL 0

Bit	Default	R/W	Description
7-0	100	R/W	Display window left 7-0 in VGA pixel coordinates

Display Window Right A (B4h)

7	6	5	4	3	2	1	0
DWR 7	DWR 6	DWR 5	DWR 4	DWR 3	DWR 2	DWR 1	DWR 0

Bit	Default	R/W	Description
7-0	164	R/W	Display window right 7-0 in VGA pixel coordinates

Display Window Left/Right B (B5h)

7	6	5	4	3	2	1	0
DWL 10	DWL 9	DWL 8			DWR 10	DWR 9	DWR 8

Bit	Default	R/W	Description
2-0	1	R/W	Display window right 10-8 in VGA pixel coordinates
2-0	0	R/W	Display window left 10-8 in VGA pixel coordinates

Display Window Top A (B8h)

7	6	5	4	3	2	1	0
DWT 7	DWT 6	DWT 5	DWT 4	DWT 3	DWT 2	DWT 1	DWT 0

Bit	Default	R/W	Description
7-0	100	R/W	Display window top 7-0 in VGA pixel coordinate

Display Window Bottom A (BCh)

7	6	5	4	3	2	1	0
DWB 7	DWB 6	DWB 5	DWB 4	DWB 3	DWB 2	DWB 1	DWB 0

Bit	Default	R/W	Description
7-0	84	R/W	Display window bottom 7-0 pixel coordinate

Display Window Top/Bottom B (BDh)

7	6	5	4	3	2	1	0
DWT 9	DWT 8					DWB 9	DWB 8

Bit	Default	R/W	Description
1-0	1	R/W	Display window bottom 9-8 in VGA pixel coordinate
7-6	0	R/W	Display window top 9-8 VGA pixel coordinate

Output Vertical Zoom Control A (C0h)

7	6	5	4	3	2	1	0
OVZC 7	OVZC 6	OVZC 5	OVZC 4	OVZC 3	OVZC 2	OVZC 1	OVZC 0

Bit	Default	R/W	Description

7-0	0	R/W	Vertical zoom factor The vertical zoom factor is specified as the numerator of a fraction with a denumerator of 2048. The vertical zoom factor is the ratio between the view port height and the display window height. It is similar to specifying the size of a step in the view port when the output advances one step.

Output Vertical Zoom Control B (C1h)

7	6	5	4	3	2	1	0
					OVZC 10	OVZC 9	OVZC 8

Bit	Default	R/W	Description
2-0	4	R/W	Vertical zoom factor

Output Horizontal Zoom Control A (C4h)

7	6	5	4	3	2	1	0
OHZC 7	OHZC 6	OHZC 5	OHZC 4	OHZC 3	OHZC 2	OHZC 1	OHZC 0

Bit	Default	R/W	Description
7-0	0	R/W	Horizontal zoom factor The vertical zoom factor is specified as the numerator of a fraction with a denumerator of 2048. The vertical zoom factor is the ratio between the view port height and the display window height. It is similar to specifying the size of a step in the view port when the output advances one step.

Output Horizontal Zoom Control B (C5h)

7	6	5	4	3	2	1	0
					OHZC 10	OHZC 9	OHZC 8

Bit	Default	R/W	Description
2-0	4	R/W	Horizontal zoom factor

Vertical Coordinate Offset (C6h)

7	6	5	4	3	2	1	0
VCO 7	VCO 6	VCO 5	VCO 4	VCO 3	VCO 2	VCO 1	VCO 0

Bit	Default	R/W	Description
7-0	-	R	Vertical coordinate offset These bits shows the internal line count at the first non-blank pixel of each vga frame. These bits are updated at the first non-blank vga pixel after every vsync. Software should read these bits at the trailing edge of blank (when blank changes from low to high.)

Horizontal Coordinate Offset (C7h)

7	6	5	4	3	2	1	0
HCO 7	HCO 6	HCO 5	HCO 4	HCO 3	HCO 2	HCO 1	HCO 0

Bit	Default	R/W	Description
7-0	-	R	Horizontal coordinate offset These bits shows the internal pixel count at the first non-blank pixel of each vga frame. These bits are updated at the first non-blank vga pixel after every vsync. Software should read these bits at the trailing edge of blank (when blank changes from low to high.)

GPO Data 0 (CBh)

7	6	5	4	3	2	1	0
GPOD R3	GPOD R2	GPOD R1	GPOD R0	GPOD G5	GPOD G4	GPOD G3	GPOD G2

Bit	Default	R/W	Description
7-0	0	R/W	General purpose output data When the output data muxing is enabled, the output pins R(3:0) and G(5:2) follow these register bits.

GPO Data 1 (CCh)

7	6	5	4	3	2	1	0
RDAC CMD						GPOD R5	GPOD R4

Bit	Default	R/W	Description
1-0	00	R/W	General purpose output data When the output data muxing or 16 bit (565) output mode is enabled, and RAMDAC command is disabled, the output pins R(5:4) follow these register bits.
7	1	R/W	RAMDAC command enable 0 - Disable 1 - Enable When output data muxing or 16 bit (565) output mode is enabled, and RAMDAC command control is enabled, red(5) become the ramdac_cs signal. Red(4) outputs the GPODATA(R4) value. Ramdac_cs is active for IOW to addresses X3C6-X3C9, where X are the four palette address bits defined in the Palette Control Register. If RAMDAC command is disabled, red(5) outputs the GPODATA(R5) value. NOTE : RAMDAC command is alway enabled when por(10) = '0'.

VGA Control C (CDh)

7	6	5	4	3	2	1	0
	CLKS 1	CLKS 0	RCD 3	RCD 2	RCD 1	RCD 0	PWC EN

Bit	Default	R/W	Description
0	0	R/W	Pulse width compensation 0 - Low pulse width compensation 1 - High pulse width compensation
4-1	2	R/W	System VGA clock rising edge delay 0 - -4 delays 4 - 0 delays 14 - 10 delays 15 - stop clock Each delay is approximately 1 ns. Delay is relative to the delayed data. When the clock is stopped, some of the registers may not be be functional.
6-5	0	R/W	System VGA clock select 00 - Delayed clock (vga_clock_in signal delayed by bit 4:1 setting) 01 - Undelayed clock (use straight vga_clock_in) 10 - Inverted delayed clock 11 - Delayed clock with pulse width compensation with delay (high or low pulse width compensation as specified in bit 0)

VGA Control D (CEh)

7	6	5	4	3	2	1	0
BK S1	BK S0		FCD 3	FCD 2	FCD 1	FCD 0	FCI

Bit	Default	R/W	Description
0	0	R/W	System VGA clock falling edge invert 0 - non-inverted clock 1 - inverted clock
4-1	4	R/W	System VGA clock falling edge delay 0 - -4 delays 4 - 0 delays 14 - 10 delays 15 - stop clock Each delay is approximately 1 ns.
7-6	1	R/W	VGA blank sample delay 0 - -1 clock 1 - 0 clock 2 - 1 clock 3 - 2 clock

Max Hcount1 (D0h)

7	6	5	4	3	2	1	0
MH 7	MH 6	MH 5	MH 4	MH 3	MH 2	MH 1	MH 0

Bit	Default	R/W	Description
7-0	-	R	Maximum number of horizontal pixels per line This value is used by software to calculate viewport left origin to allow video frame wraparound on the left edge of the vga window.

Max Hcount2 (D1h)

7	6	5	4	3	2	1	0
					MH 10	MH 9	MH 8

Bit	Default	R/W	Description
2-0	-	R	Maximum number of horizontal pixels per line. This value is used by software to calculate viewport left origin to allow video frame wraparound on the left edge of the vga window.

Interrupt Control (D2h)

7	6	5	4	3	2	1	0
						VSIE	HSIE

Bit	Default	R/W	Description
0	0	R/W	Horizontal sync interrupt enable 1 - Enable 0 - Disable When set an interrupt is generate at the beginning of a vga horizontal sync.
1	0	R/W	Vertical sync interrupt enable 1 - Enable 0 - Disable When set an interrupt is generate at the beginning of a vga vertical sync.

Interrupt Status (D3h)

7	6	5	4	3	2	1	0
		VSIS	HSIS	UFLW	BS	VS	HS

Bit	Default	R/W	Description
0	-	R	Horizontal sync 1 - HS active 0 - HS inactive This signal shows the state of the vga horizontal sync signal.
1	-	R	Vertical sync 1 - VS active 0 - VS inactive This signal shows the state of the vga vertical sync signal.
2	-	R	Blank status 1 - blank inactive 0 - blank active This signal shows the state of the vga blank signal.
3	-	R	Underflow indicator 1 - the fifo has underflowed since the last time this register has been read. 0 - no underflow This bit clears after INT_STATUS has been read.
4	-	R	Horizontal sync interrupt status 1 - interrupt caused by horizontal sync 0 - interrupt not caused by horizontal sync This signal is cleared on read.

5	-	R	Vertical sync interrupt status 1 - interrupt caused by vertical sync 0 - interrupt not caused by vertical sync This signal is cleared on read.

VGA Data Byte 0 (D5h)

7	6	5	4	3	2	1	0
VGAD 7	VGAD 6	VGAD 5	VGAD 4	VGAD 3	VGAD 2	VGAD 1	VGAD 0

Bit	Default	R/W	Description
7-0	-	R	VGA data byte 0 These bits contains the first VGA pixel received after blank.

VGA Data Byte 1 (D6h)

7	6	5	4	3	2	1	0
VGAD 15	VGAD 14	VGAD 13	VGAD 12	VGAD 11	VGAD 10	VGAD 9	VGAD 8

Bit	Default	R/W	Description
7-0	-	R	VGA data byte 1 These bits contains the first VGA pixel received after blank.

VGA Data Byte 2 (D7h)

7	6	5	4	3	2	1	0
VGAD 23	VGAD 22	VGAD 21	VGAD 20	VGAD 19	VGAD 18	VGAD 17	VGAD 16

Bit	Default	R/W	Description
7-0	-	R	VGA data byte 2 These bits contains the first VGA pixel received after blank.

Chroma Key Red Low (D8h)

7	6	5	4	3	2	1	0
CKRL 7	CKRL 6	CKRL 5	CKRL 4	CKRL 3	CKRL 2		

Bit	Default	R/W	Description
7-2	0	R/W	Chroma key red low value

Chroma Key Red High (D9h)

7	6	5	4	3	2	1	0
CKRH 7	CKRH 6	CKRH 5	CKRH 4	CKRH 3	CKRH 2		

Bit	Default	R/W	Description
7-2	3F	R/W	Chroma key red high value

Chroma Key Green Low (DAh)

7	6	5	4	3	2	1	0
CKGL 7	CKGL 6	CKGL 5	CKGL 4	CKGL 3	CKGL 2		

Bit	Default	R/W	Description
7-2	0	R/W	Chroma key green low value

Chroma Key Green High (DBh)

7	6	5	4	3	2	1	0
CKGH 7	CKGH 6	CKGH 5	CKGH 4	CKGH 3	CKGH 2		

Bit	Default	R/W	Description
7-2	3F	R/W	Chroma key green high value

Chroma Key Blue Low (DCh)

7	6	5	4	3	2	1	0
CKBL 7	CKBL 6	CKBL 5	CKBL 4	CKBL 3	CKBL 2		

Bit	Default	R/W	Description
7-2	0	R/W	Chroma key blue low value

Chroma Key Blue High (DDh)

7	6	5	4	3	2	1	0
CKBH 7	CKBH 6	CKBH 5	CKBH 4	CKBH 3	CKBH 2		

Bit	Default	R/W	Description
7-2	3F	R/W	Chroma key blue high value

3.0 Register User's Guide

3.1 General Registers

From a software point of view, VxP202 appears as two 16/8 bit ISA I/O ports and a 16 bit memory map. VxP202's registers provide controls, status, and access to the data path. Its memory map also provides access to the data path. Figure 3.1.0 is a simplified block diagram for the VxP202.

The two I/O ports act as an index register and a data register. The index register is used to point to any VxP202 register that the software wants to access. The data register port is used to read and write data to the register that the index register points to. At power up, hardware reserves 4 ISA I/O ports: index register and data register which can both be 16 bits. VxP202's I/O port address bits 15 to 10 are fixed as 00 0001b. Only bits 9 to 2 are programmable at power up.

As an example, assume that ISA I/O ports 0640 and 0642 are selected as register index port and register data port respectively. To read from the Refresh Count Register (index = 12h), first write 12h (index) to ISA port 0640h (index register). Next, read from ISA port 0642h (data register). The contents of ISA port 0642h will be the contents of the Refresh Count Register.

To write to the Horizontal Filter Mode Select Register (index = 50h), first write 50h (index) to ISA port 0640h (index register). Next, write to ISA port 0641h (data register). The value written to ISA port 0641 will be placed into the Horizontal Filter Mode Select Register.

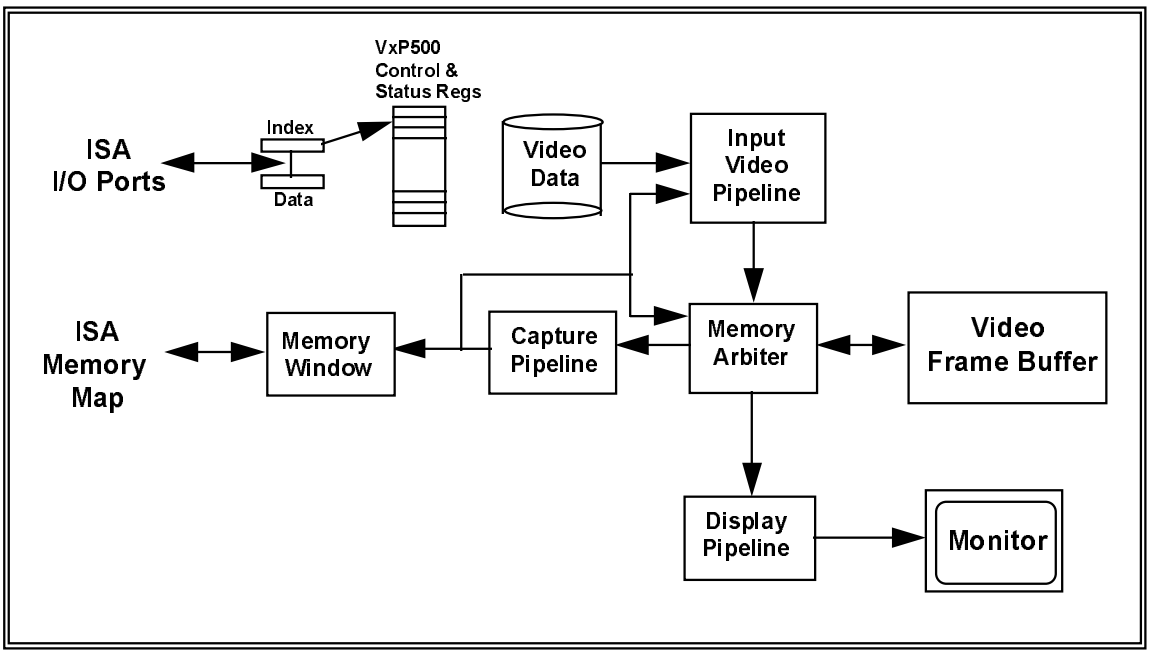


Figure 3.1.0 VxP202 Software Model

Access To Registers

Before registers can be accessed the IO Base Address register must contain a value other than "FF" hex. The IO Base Address register section describes how to program this register. Once programmed, an index and data register will be mapped on 16-bit boundaries at an IO Address that is derived from the value in the IO Base Address register. The index register is a 16-bit register and can respond to 8 or 16-bit accesses. The data register may be 8 or 16 bits, depending on the index that was most recently written. The following table shows Index Space Mapping.

Register Index Range	Width	Description
0-FF	8-Bit	VxP202 Internal Registers
100-3FFF	8-Bit	External Registers
4000-7FFE	16-Bit	External Registers
7FFF	16-Bit	Programmed IO i.e. Capture/Playback i.e. PX Bus Access
8000-FFFF	16-Bit	Reserved

Table 3.1.0 Index Space Mapping

The first range, the VxP202 internal registers, hold bits that configure the internal state of the VxP202. The second and third ranges address 8 and 16-bit registers that may be set up by a board designer to configure the state of other components that share the board with VxP202. The address "7FFF" allows access to VxP202's internal PX Bus, which interconnects the Video Input Pipeline and Capture Pipeline together. For example, by programming the PX Bus Configuration Register (12h), the PX Bus can be configured to connect the ISA interface to say the Capture Pipeline. Capturing video data is then as easy as writing "7FFF" to the index register and performing IO reads from the data register.

ISA/Memory Control & Status Registers

Index	**Register Name**
10h	IO Base Address Register
11h	Power On Reset Register
12h	PX Bus Configuration Register
14h	Memory Window Control Register
17h	DRAM Control Register
27h, 28h	Clock Frequency Low and High Registers
30h	ISA Control Register

Table 3.1.1 Interface Registers.

10h, 11h The IO Base Address and Power On Configuration Registers

There are three ways the IO Base Address Register can be programmed. It can be set on power up by tying pull-ups and pull downs to the SASD[7:0] bus in a power on reset configuration. It can be programmed by writing to index 10h. Lastly, there is a "port 80 back door" sequence that can be performed to write to the IO Base Address register when all the SASD[7:0] lines have pull-ups.

If the SASD[7:0] lines are not all high at the trailing edge of reset, the VxP202 will respond to two IO registers. The addresses of these two registers are derived from the value stored in the IO Base Address register. If all the lines *are* high at the trailing edge, then VxP202 will not respond to any IO accesses, except to snoop during writes to port 80h.

At the falling edge of reset, the value on the entire SASD[15:0] bus is sampled and stored by the VxP202. This sampling process is called the Power On Reset sequence. The value sampled is called the Power On Reset value (POR). The lower 8 bits of the POR are stored in the IO Base Address Register while the upper 8 are stored in the Power On Reset Register.

Whenever the value "FF" hex is written to the IO Base Address register, regardless of which of the three methods were used, The VxP202 is set in a "Power On Configuration" mode where it watches writes to port 80h and does not respond to any other IO access. In Power On Configuration mode, the VxP202 waits for a code word of ASCII bytes to be written to IO port 80h. The last byte written is the IO Base Address register value. The code word is: AURAV1, F4hex, 0Bhex, <IOBA>, where <IOBA> represents the address byte. As soon as a value other than "FF" hex is written, the VxP202 leaves Power On Configuration mode and is able to respond to the Index and Data registers. The addresses for these two registers fall on 16-bit boundaries and are derived from the IO Base Address register value as follows:

Index Register:

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	1	B7	B6	B5	B4	B3	B2	B1	B0	0	0

Data Register:

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	1	B7	B6	B5	B4	B3	B2	B1	B0	1	0

B = IO Base Address register bit

12h PX Bus Configuration Register

The PX Bus is an internal VxP202 bus that interconnects the ISA interface, the Compression CODEC pixel interface and the Video Input Pipeline together. The PX Bus Configuration register defines which two devices are connected, which is the master, which direction data will flow. When a device is "master" it controls the command that causes data to pass. The "slave" controls the ready status line which informs the master whether or not the slave is ready to transfer data. Data can flow from the master to the slave or vice versa. Only some of the possible connections are allowed. See the register specification for more details. All IO, Memory, or DMA accesses are made to the VxP202 directly go through the ISA Interface. All references to the ISA Interface in the register description refer to these types of accesses.

14h, The Memory Window Control Register

The Video Input and Capture pipelines can also be accessed through a memory window on the ISA bus. Random access to the DRAM buffer is *not* supported though. The VxP202 will respond to memory reads and writes only when the address is within the range specified by the Memory Window Control Register. The Capture Pipeline

should be set up and contain data before performing memory reads. Likewise, the Video Input Pipeline needs to be set up for playback before performing memory writes. The address must be within the memory window but is ignored beyond that. In other words accesses to the same location or to successive locations have the same effect, and have no effect on the DRAM address. Address generation for DRAM is done internally to the VxP202 and is controlled by the viewport registers. The advantage to using memory accesses is that they can run using zero wait state cycles -- the fastest possible cycle. This may not necessarily mean that memory transfers are faster then IO transfers since sustained transfer rate is highly dependent on the platform bus controller. In other words the length of the cycle itself may be faster than an IO cycle but if the time between cycles is long, the average transfer rate won't be effected very much. For more details on how to program the Memory Window Control Register, see the register specification.

17h DRAM Control Register

VxP202's Memory Control Register contains three variable parameters. These are the RAS_N to CAS_N Delay (tRCD), RAS_N Pre-Charge Time (tRP) and the frequency of the memory clock. By adjusting these parameters, different types of DRAM and performance targets may be selected. The programmable range for tRCD is 2 to 4 memory clocks. The programmable range for tRP Pre-charge is 1 to 5 clocks. The memory clock frequency can vary between 50MHz and 66.67 MHz. A fourth parameter exists called tRSH. Normally this should be set to 0, but if a board designer decides to use the CAS_N signal for purposes such as memory snooping, it should be set to 1. If CAS_N is heavily loaded relative to the other memory signals, the tRSH DRAM parameter may be violated with a setting of 0.

It is very easy to determine the correct settings for any DRAM based on its specification. The memory clock period is found by dividing the tPC DRAM parameter by 3. The number of clocks allowed for tRCD is found by dividing the tRSH parameter by the memory clock period and subtracting 2. Dividing the tRP parameter by the clock period will provide the number of clocks needed for tRP. The following outline shows settings for various speeds and makers of DRAM's.

Mitsubishi 256Kx16

80 ns

Memory Clock Frequency	= 60MHz
tRCD	= 1 (3 clocks)
tRP	= 4 (5 clocks)

70 ns

Memory Clock Frequency	= 66MHz
tRCD	= 1 (3 clocks)
tRP	= 3 (4 clocks)

60 ns

Memory Clock Frequency	= 66MHz
tRCD	= 0 (2 clocks)
tRP	= 3 (4 clocks)

Mitsubishi 256Kx4

100 ns

Memory Clock Frequency = 50MHz
tRCD = 1 (3 clocks)
tRP = 3 (4 clocks)

80 ns

Memory Clock Frequency = 60MHz
tRCD = 1 (3 clocks)
tRP = 4 (5 clocks)

70 ns

Memory Clock Frequency = 66MHz
tRCD = 1 (3 clocks)
tRP = 3 (4 clocks)

Micron 256Kx16 or 256Kx4

80 ns

Memory Clock Frequency = 66MHz
tRCD = 2 (4 clocks)
tRP = 3 (4 clocks)

70 ns

Memory Clock Frequency = 66MHz
tRCD = 1 (3 clocks)
tRP = 3 (4 clocks)

60 ns

Memory Clock Frequency = 66MHz
tRCD = 0 (2 clocks)
tRP = 2 (3 clocks)

NEC 256Kx16

80 ns

Memory Clock Frequency = 60MHz
tRCD = 1 (3 clocks)
tRP = 3 (4 clocks)

70 ns

Memory Clock Frequency = 66MHz
tRCD = 1 (3 clocks)
tRP = 3 (4 clocks)

70 ns

Memory Clock Frequency = 66MHz
tRCD = 0 (2 clocks)
tRP = 3 (4 clocks)

NEC 256Kx4

100 ns

Memory Clock Frequency	= 50MHz
tRCD	= 1 (3 clocks)
tRP	= 3 (4 clocks)

80 ns

Memory Clock Frequency	= 60MHz
tRCD	= 1 (3 clocks)
tRP	= 4 (5 clocks)

70 ns

Memory Clock Frequency	= 66MHz
tRCD	= 1 (3 clocks)
tRP	= 3 (4 clocks)

60 ns

Memory Clock Frequency	= 66MHz
tRCD	= 0 (2 clocks)
tRP	= 3 (4 clocks)

There is an additional field in the Memory Control Register called Refresh Enable. By negating the refresh enable bit, VxP202 will disable all video frame buffer refresh cycles. The frame buffer DRAM will have to rely on normal memory access for memory retention. It will have unpredictable results on stored frame buffer data.

A request for refresh will occur every 768 memory clocks. If the memory controller is busy servicing a request from one of the three pipelines, the request will be ignored. A "refresh pending" counter will increment though. As soon as the refresh request is acknowledged, a burst of refreshes will occur -- one for every previously ignored request.

27h, 28h, The Clock Frequency Low and High Registers

These registers control two counters. One increments for every memory clock. The other increments for every clock of the selected clock, the choice being between the video input and video output clocks. After the counting completes, the value in the Clock Frequency Registers will reveal the frequency of the selected clock based on the following formula:

$$f = 256 \cdot f_M / COUNT$$

The f_M parameter represents the memory clock frequency and COUNT represents the value read from the two registers.

Finding the frequencies of the video input and video output clocks is important in order to determine bandwidth requirements for DRAM access.

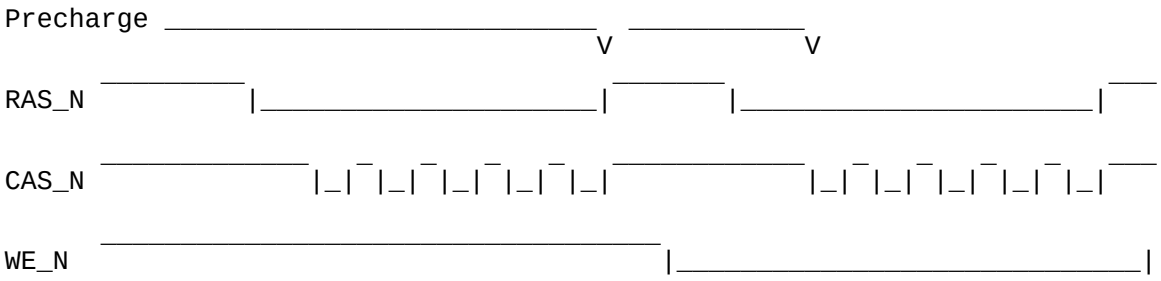
30h, The ISA Control Register

This register holds various mode bits that will configure the ISA bus interface and internal state of the VxP202. For further details, see its description under the register specification.

Bandwidth to DRAM

In General

In order to understand issues concerning DRAM bandwidth, an understanding of the signals and timing is required. The following is a rough illustration of DRAM timing.



This timing shows a burst of read cycles followed by a burst of writes. A new word of data is read or written for every low to high transition of the CAS_N signal. There are at most 3 data streams that can be active at a time, namely the Video Input, the Capture and the Video Output streams. They are controlled by their respective pipelines. The 3 pipelines take turns accessing DRAM, and use FIFOs for queuing data when they wait.

Traffic Analogy

The process is very similar to a traffic intersection. The light turns green in one direction and allows a stream of traffic though while the other stream waits and allows cars to queue. The longer the light stays green for one direction, the more cars accumulate in the other direction. Time is waisted during the transition, but is made up for by long traffic bursts in each direction.

You can think of the average "bandwidth" for the intersection as the average number of cars to cross per second. When the light turns green in one direction and the traffic is allowed to reach its highest speed, the peak bandwidth will be reached. The overall bandwidth can be thought of as some percentage of this peak number. We'll call this percentage weighting factor the "transfer efficiency".

An intersection can range from a 4-way stop, where cars alternate, to an intersection with a very long traffic light. The 4-way stop intersection is the least efficient. The longer the light the closer the transfer efficiency comes to 100%. The trade-off is the maximum build-up of cars in the stopped direction, since this increases as the light duration increases.

This maximum car build-up is analogous to the VxP202's FIFO depths, while the transition time is analogous to the "Precharge" that is shown in the above timing diagram. 85% is a typical transfer efficiency for the VxP202 when all pipelines are operating. The bandwidth can be calculated using the following formula:

Bandwidth = (transfer efficiency) * (interleave) / (3 * memory clock period)

This follows from:

Bandwidth = (number of pixels transfered) / (time it took to transfer them)

For example, with an efficiency of 85%, an interleave of 2 and a 66MHz memory clock, the bandwidth would be around 37.8 Mpps (Mega Pixels Per Second).

Calculating Q-factor:

The VxP202 was designed to operate at pipeline data rates beyond the DRAM bandwidth capability. The chip allows this by controlling data flow through the DRAM data port. The measure of the degree at which this occurs is called the Q-factor. As you read other sections, you may have discovered that video can be scaled and zoomed. The two processes can operate simultaneously. In other words, video can be scaled and zoomed at the same time.

The horizontal scaling process is controlled by the video input pipeline and eliminates pixels before they are written to DRAM. The horizontal zooming process is controlled by the video output pipeline and duplicates pixels after they are read from DRAM. Each of these processes has the effect of decreasing the data flow rate of it's respective stream. Pixels flow into the video input pipeline at a rate equal to its clock frequency. Yet only a percentage (equal to the horizontal scale factor) pass through. The rest are discarded. Likewise, pixels flow out of the video output pipeline at a rate equal to the video output clock or VGA Feature Connector clock. Yet, a group of pixels that are read by the video output pipeline represents only a percentage (equal to the horizontal zoom factor) of the pixels that are actually displayed. The rest are duplicated. The displayed image will not be distorted (stretched or compressed) if the horizontal scale and zoom registers are decreased proportionally, but the data flow to DRAM will decrease dramatically. Please refer to the Horizontal Scaling Control registers (54h and 55h) and the Output Horizontal Zoom Control registers (C4h and C5h) for more details on scaling and zooming. Q-factor adjustments like this result in a slight increase in "graininess" of the image. Bandwidth is only effected by horizontal controls since that is the dimension that drives peak bandwidth.

Usign Pixel Drop Feedback to Determine Q-Factor

The VxP202 must overlay video onto a graphics window and the video must conform to any rectangular dimensions that the user specifies with the screen size limits. This means that video may be required to be scaled for one rectangle or zoomed for another. The value of the scale or zoom factor may take on a full range of values. For bandwidth, we are only concerned with the horizontal dimension, and it is easier to think of it in terms of an over-all weighting factor that will be less than 1.0 for scaling and greater than 1.0 for zooming. We'll call it "Z". For example, for a Z=0.5, the display dimension will be half that of the

incoming video dimension, and the scale factor register (call it A) may be set to 0.5 (its binary equivalent). For a Z=2.0, the screen dimension will be twice that of the incoming video dimension, and the zoom factor register (call it B) may be set to 0.5 (in binary). Another way to achieve a Z = 2.0 would be to set A = 0.75 and B = 0.375. The formulas to determine these factors is as follows:

$$B = A/Z$$

$$A = Z*B$$

Which are easily found from the definition of Z, namely:

$$Z = A/B$$

As long as "A" and "B" change proportionally (say by a factor of "q"), Z will not change. Let "a" and "b" represent initial estimates for horizontal scale zoom factors resepctively. If "A" and "B" parameters will still represent what is written to the scale and zoom registers, then the factor "q" can be chosen such that:

$$A = q*a$$
$$B = q*b$$

As "q" varies bandwidth will change but "Z" will not:

$$Z = A/B = (q*a) / (q*b) = a/b$$ no matter what q is.

If a very small "q" is chosen, then the bandwidth requirement will be very low. As "q" increases, bandwidth requirement will also increase. Bit 5 of the Interrupt Control register (60 hex) is the "FIFO Drop" status bit which indicates whether or not the Video Input FIFO has dropped any pixels. The FIFO will do this only when bandwidth has run out. A software routine can use this bit as a feedback mechanism to determine when "q" crosses the maximum bandwidth boundary.

Weighting Factor and Formulas

The bandwidth that a stream requires is easily calculated as follows:

$ß_i = A * F_i$
$ß_o = B * F_o$
$ß_{hc} = F_m / 4$

$ß_i$ = Video Input Bandwidth
$ß_o$ = Video Output Bandwidth
$ß_{hc}$ = Hardware Capture Bandwidth (CODEC Capture)
$ß_c$ = Capture Bandwidth in general (either CODEC or software capture)

F_i = Video Input Clock Frequency
F_o = Video Output Clock Frequency
F_m = Memory Clock Frequency

The software capture bandwidth is highly platform and software dependent, and is therfore not shown above. The following is the bandwidth formula that must be satisfied every time the horizontal constraints must be re-calculated:

$ß_m = ß_i + ß_c + ß_o$

The following is the formula described previously:

$ß_m$ = (transfer efficiency) * (interleave) / (3 * memory clock period)

If bandwidth were not an issue, then either A or B would be set to 1.0 (horizontal factor disabled) while the other was set to the appropriate factor. Bringing bandwidth back into consideration, a Q-factor adjustment could be made to restrict data flow. Let's say a scale factor of "a" and a zoom factor of "b" were picked this way. The A and B register settings could then be calculated by determining "Q", the Q-factor as follows:

A = Q * a
B = Q * b

Since:

Z = A/B

It follows that:

Z = (Q*a)/(Q*b)

So:

Z = a/b

And:

a = Z*b
b = a/Z

Q can be found by solving this formula for Q:

If a = 1.0 then

$ß_m = (Q * 1.0) * F_i + ß_c + (Q * [1.0/Z]) * F_o$

Knowns: $ß_m$, $ß_c$, F_i , F_o , Z
Unknown: Q

If b = 1.0 then

$ß_m = (Q * [Z*1.0]) * F_i + ß_c + (Q * 1.0) * F_o$

Knowns: $ß_m$, $ß_c$, F_i , F_o , Z
Unknown: Q

Another way to look at the problem is to forget Q completely and calculate A and B directly from the following:

$ß_m = A * F_i + ß_c + (A/Z) * F_o$
Knowns: $ß_m$, $ß_c$, F_i , F_o , Z
Unknown: A

B = A/Z

To find Q using this method, remember that:

A = Q * a
B = Q * b

And either a or b is equal to 1.0. This means that if A > B then Q=A, otherwise Q=B.

An Example

For example, assume that an NTSC Decoder is driving the video input pipeline of the VxP202 and the horizontal active line width is 640. The video input clock was measured to be 13MHz. If the VGA is in 1024X768 mode, the VGA clock might be measured to be 45MHz. A user stretches the window horizontally and drops it so the display width is 960 pixels. The interleave factor is 2, since the DRAM width is 16-bits and data is stored in 422 compressed format. The memory clock is 50MHz. Hardware capture will be running. The horizontal scale and zoom registers now need to be set so that they satisfy the horizontal dimension and the bandwidth requirements.

$ß_m = A * F_i + ß_c + (A/Z) * F_o$

$A = (ß_m - ß_c) / (F_i + F_o/Z)$

Z = 960pixels / 640pixels = 1.5

A = [0.85 * 2pixels / (3*20ns) - (12.5Mpps)] / (13MHz + 45MHz / 1.5)

A = 0.368 pixels per cycle (ppc)

B = 0.368 / 1.5 = 0.245 ppc

Double Checking:

Z = A/B = 0.368/0.245 = 1.5

$ß_m = ß_i + ß_c + ß_o$

0.85 * 33.3Mpps = 13MHz * 0.368 ppc + 50MHz / 4 cpp + 45MHz * 0.245 ppc

28.33 Mpps = 28.33 Mpps

3.2 Video-In Register

Video Input Pipeline Registers

Index	Register Name
34h	I^2C Control
36h - 37h	PLL Control A & B
38h - 39h	Input Video Configuration A & B
3Ah - 3Bh	ISA Source Window Width A & B
3Ch - 3Dh	ISA Source Window Height A & B
40h - 41h	Input Horizontal Cropping Left A & B
44h - 45h	Input Horizontal Cropping Right A & B
48h - 49h	Input Vertical Cropping Top A & B
4Ch - 4Dh	Input Vertical Cropping Bottom A & B
50h	Input Filter Control
54h - 55h	Input Horizontal Scaling Control A & B
5Bh - 5Ch	Input Vertical Scaling Control A & B
5Dh, 5Eh, 5Fh	Picture Control address and data registers
60h	Video Input Interrupt Control
61h	Video Input Interrupt Status
68h	Video Input Frame-Buffer (Multi-Buffer) Depth Control A
6Dh	Video Input Time Scaling Control
73h	Video Buffer Layout Control
78h	Input FIFO Low & High Marker

Table 3.2.0

These registers should not be changed on the fly. They should be programmed during software reset or global reset.

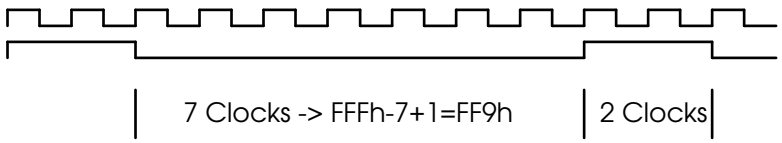
34h I2C Control Register

The I^2C control register provides access to the I^2C bus. VxP202 does not provide the I^2C bus controller function, however it allows software to emulate the I^2C bus controller function. Bits (6-0) of this register allow software to control as well as read back the state of the two I^2C signals, data and clock. Bits (3-0) are readable and writeable, bits (6-4) are readable only. Bit 7 of this register serves as the I^2C frame bit when the bits defining the pulse width of the PLL clock (bits 4-7, 37h) are all '0'. Otherwise this bit is used as a feedback for the PLL clock divider. This register can be altered at anytime, reset is not required.
Note: the speed of the I^2C bus does not require the use of a hardware controller.

36h, 37h PLL Control Registers

The PLL control registers provide the values for the clock divider and the clock pulse width for the Phase Lock Loop. The PLL Control register A (36h) contains the low byte value of the clock divider. Bits (3-0) of the PLL register B (37h) contain the high byte value of the clock divider. The remaining bits of this register (7-4, 37h) specify the pulse width of the clock. When these four bits are "0000" then the I2C_FRAME pin is sourced from bit(7) of the I^2C register . Otherwise, the I^2C_FRAME pin is sourced by the PLL clock divider. The PLL clock divider generates a periodic pulse from the VINCLK. The following figure illustrates how to program these registers correctly. The inactive time is determined by an incrementing counter. The register sets the initial value. Then when there is a carry the pulse begins. Therefore if a pulse inactive period of 7 clocks is desired, the register should be programmed with FFFh-7+1=FF9h. The pulse width is the width of the pulse itself. Therefore a pulse

width of 0 is illegal and can be used to disable the pulse generator. This register may be altered at anytime, reset is not required.



38h,39h Input Video Configuration Registers

The Input Video Configuration registers control VxP202's input video processing functions. The Input Configuration A register can be programmed to select the vertical and horizontal sync polarity, to enable the input video decoder, to reset the input pipeline, and to enable the test mode for the picture control RAMs. The Input Configuration B register provides the input data format, the video scan type, the memory data type, and selects the input video sources.

Input Configuration A Register (38h)

VSYNC/HSYNC POL (bits 1-0)
These bits select the active polarity for VSYNC and HSYNC

E_SYNC (Early Sync)
In a typical system, Horizontal and Vertical Sync are referenced to the input video data. In systems which support pixel tagging, a pixel tag can appear one cycle before or coincide with pixel data. In the case where pixel tag is one clock cycle (pixel clock) earlier than pixel data, Horizontal and Vertical Sync may be referenced to the pixel tag. By setting the E_SYNC field to 1, VxP202 can accept early Sync. Note: refer to your system specification for proper setting.

VIDE (video decoder/CL450 enable)
This field turns on the video decoder input. Software reset does not have to be active to toggle this bit. When this bit is changed from 0 to 1, the input searches for a start of an even field before activating the input decoder. Likewise, when this bit is changed from 1 to 0, the input waits until the start of an even field before turning the input decoder off. This guarantees a clean data stream in the input pipeline.

RST - Input pipeline reset
Writing a '1' to this field activates software reset for the input pipeline; writing a '0' will clear the software reset. When this bit or global reset (bit 7, 30h) is set, the input pipeline will be inactive; However, the registers are not reset. This bit must be active while any input register is being programmed, except the VIDE bit (bit3, 38h) in the input configuration A register.

DLY_HSYNC
Setting this bit to '1', the internal HSYNC is delayed one clock cycle, in turn the UV group can be swapped. This allows more flexibilty for the VxP202 to interface with the external video decoder.

TEST_COMP/TEST_RAM (bit 7-6, 38h)
These two bits control the test mode for the palette RAMs (two 256x8 RAMs in the picture control block). If the programmed value of these two bit is either '01' or '11', then the RAM's test mode is enable. And all RAM's locations will be written with test data of "55" (for '01') or "AA" (for '11') .

Input Configuration B Register (39h)

DAT_FMT1/DAT_FMT0 - Input data format
These two bits select the input data format from the four allowable input formats: YUV 4:2:2, RGB 5:5:5, RGB 5:6:5 or Palettized data.

CPS_EN - Compressed buffer enable

VXP202 supports 6-bit or 8-bit per pixel compressed formats or 16-bit YUV 4:2:2 uncompressed format. When this field is set to ’1’ , the input data is compressed, otherwise the uncompressed, 16-bit YUV data will be used.

INTLCN
VXP202 supports both interlaced and progressive (non-interlaced) video input. This bit selects whether the input is interlace or progressive. If the input is interlace and this bit is set to progressive, then each field is treated as an independent frame. ISA playback is usually progressive, but in the case of HWPB the input may be interlace. The first field after reset is considered to be an even field.

DIFF_FMT - Memory data type
This bit selects the compressed data type of the memory : 6-bit 4:1:1 differential data or 8-bit 4:2:2 differential data.

VIO_VIN_N
This bit selects the input source for live video and hardware playback. Writing a ’0’ to this bit will select video decoder, writing a ’1’ will select hardware playback with C-Cube CL450.
Note: software playback is played through host ISA bus.

MEM_MODE	Input Type	Buffer Type	Configuration B
8 or 16 bit	YUV422	Comp422	XXX1X100
8 or 16 bit	YUV422	Comp411	XXX0X100
8 or 16 bit	YUV422	Uncompressed	XXXXX000
8 or 16 bit	RGB15	Comp422	XX01X101
8 or 16 bit	RGB15	Comp411	XX00X101
8 or 16 bit	RGB15	Uncompressed	XX0XX001
8 or 16 bit	RGB16	Comp422	XX01X110
8 or 16 bit	RGB16	Comp411	XX00X110
8 or 16 bit	RGB16	Uncompressed	XX0XX010
8 or 16 bit	Palettized	Comp422	XX01X111
8 or 16 bit	Palettized	Comp411	XX00X111
8 or 16 bit	Palettized	Uncompressed	XX00X011
8 bit	Comp422	Comp422	XX01X011
8 bit	Comp411	Comp411	XX01X011
16 bit	Comp422	Comp422	XX0XX000
16 bit	Comp411	Comp411	XX0XX000

3Ah, 3Bh, 3Ch, 3Dh ISA Source Window Height and Width Registers

These registers define the height and the width of the ISA video input. The programmed value should be one (pixel or scan line) less than the actual width and height.

5Dh, 5Eh, 5Fh Picture Control RAM address and data registers

In the VxP202 there are two 256x8 on-chip RAMs for picture control and AVI pallettized data decoding.

These RAMs can be used as color look up RAMs to perform picture control functions including brightness, saturation, hue and contrast controls. When used in this mode, the output format for the picture control RAMs is YUV 4:2:2 excess 128. The RAMs can be accessed by writing to the index register 5Dh the RAMs address, and reading or writing registers 5Eh or 5Fh for the luma or chroma data.

If the input data is in palettized format, then the RAMs are used as palette RAMs. They decode the palettized data into RGB 5:6:5 format which is then converted to YUV 4:2:2 format through the Color Space Converter. The data in register 5Eh is R(4:0) and G(5:3). The data in register 5Fh is G(2:0) and B(4:0).

Initialization and programming the RAMs should be done during software reset when the input pipeline is not active. The RAMs are accessed with one index register (5Dh) and a pair of data registers (5Eh & 5Fh, one for each RAM).

Video Input Frame Buffer Setting, Filtering, Scaling , Cropping and Acquisition Start Address Registers

Video frame buffer setting, filtering, scaling, cropping and acquiring are all interdependent functions. In a normal acquisition sequence, the size and the configuration of the video frame buffer is set. In the cases of ISA input source, the width and the height of the ISA window also need to be defined. With decoded video, the incoming horizontal and vertical Sync defines the input window size. Next, the cropping, scaling and filtering is set. The cropping function is relative to the incoming video source. The scaling and filtering are done after croppping. In the VxP202 the acquisition starting address which is referenced to the frame buffer is always set at (0,0). Once this is accomplished, VxP202 is ready to acquire input video. During acquisition, the filtering, cropping, and scaling are performed. Figure 3.2.0 is a conceptual model for video acquisition.

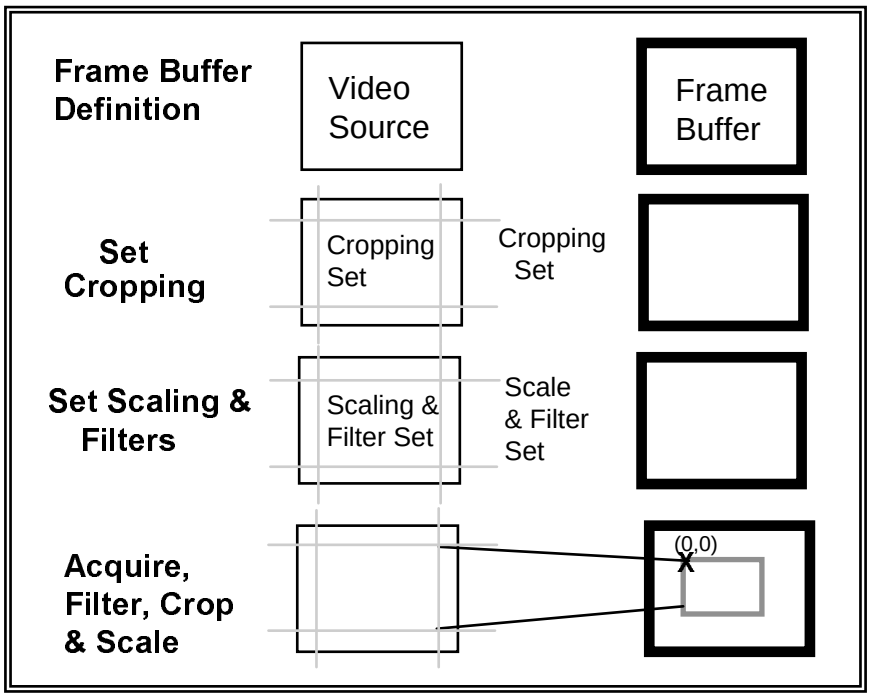


Figure 3.2.0 Acquisition Conceptual Model

Frame Buffer Definition:

Each DRAM configuration supports a number of frame buffer sizes, configurations and interleave factors. Depending on system DRAM configuration and the number of bits per pixel, the possible frame buffer sizes and configurations differ (See Table 3.2.1).

73h, Video Buffer Layout Control Register

To define the frame buffer size configuration and size, first determine the DRAM configuration and bits per pixel. Refer to your system specification. Next program the Video Buffer Layout Control Register (73h) and select the final frame buffer configuration and size. Refer to table 3.2.2.

DRAM Configuration	Bits per Pixel	Single Buffer	Double Buffer	Quad Buffer
256K x 8	6	(1.33x512)x512 (1.33x256)x1024	(1.33x256)x512	(1.33x256)x256
256K x 8	8	512x512 256x1024	256x512	256x256
256K x 16	6	(2.66x512)x512 (2.66x256)x1024	(2.66x512)x256	(2.66x256)x256
256K x 16	8	(2x512)x512 (2x256)x1024	(2x512)x256	(2x256)x256
256K x 16	16	512x512 256x1024	512x256	256x256

Table 3.2.1 Frame Buffer Size and Configuration Selection Table

VID_LAYO	
00	Select 512 Scan Line Single Buffer Configuration
10	Select 1024 Scan Line Single Buffer Configuration
01	Select Double Buffer Configuration
11	Select Quadruple Buffer Configuration

Table 3.2.2

Each of the three video frame buffer configurations has different display and capture characteristics. The single buffer configuration provides the largest display window for a given memory size. However it can only be used for still frame acquisition.

The double buffer configuration allows buffer updates on one buffer while the display reads from the second buffer. This eliminates any problems derived from overlapping update and display lines. Due to the compressed buffer architecture of the VxP202, the crossing of read and write pointers in a single buffer is catastophic. Therefore all live video should use dual or quad buffer modes.

The quadruple buffer configuration, in addition to solving the foregoing update problems, also provides more efficient video capture performance. By allowing a larger buffer space between capture and video update scan line, non-uniform data transaction can be accommodated without the loss of any video data. For example, in a normal capture sequence, the writing of video data to system memory or from system memory to hard disk are non-uniform. This is due to disk sector seek time and other ISA bus activities. In a double buffer configuration, if input video data has filled up one buffer before VxP202 can write all the video data from the second buffer to system memory (i.e. due to abnormal ISA activities), there will be no room to put the next frame of video input data. To avoid capturing frames out of sequence, VxP202 will drop a frame of video data. The quadruple buffer allows two more additional buffers thus reducing the chance of dropping video data caused by non-uniform data transaction.

Another advantage of the quadruple buffer configuration is that it allows a more efficient use of the limited ISA bandwidth. For example: When a hard disk is ready for data transfer (after a sector seek), the ISA bus may be assigned for disk data transfer (from memory to the hard disk). When a sector of disk data transfer is completed, the

ISA bus may then be assigned to the VxP202 for memory transfer (during the next hard disk sector seek). Without the additional buffering space, video frames may have to be dropped, while disk data is still being transfer in the ISA bus. By allowing the hard disk to have the ISA bus when it is required, maximum disk data throughput can be achieved.

The single buffer configuration provides the best memory efficiency for still or slow transition video. However, for video that has dramatic contrast transition from frame to frame, the visual artifacts caused by overlapping update and display may be unacceptable. At the expense of video window size, the quadruple frame buffer provides the best capture and visual performance. In most capture applications, other hardware restrictions (i.e., hard disk) normally limit the capture window to be 320 x 240 or smaller. This requirement is supported in VxP202's quadruple buffer mode in both 8-bit and 16-bit memory configurations with the interleave factors of 1.33 and 2. VxP202 allows software to change to any of the three video frame buffer configurations thus providing the optimum performance for any given applications.

68h, 8Ah, 93h Video Input, Capture and Display Frame-Buffer (Multi-Buffer) Depth Registers

To provide additional buffering space between the updating scan line and the capture scan line, VxP202 provides an active depth control feature which allows video update on a currently active buffer without causing update and display overlaps. A user programmable video depth marker is assigned to each of the three video pipelines, Video Input, Capture and Display. Once the depth marker has been reached, the frame buffer is freed and treated as a non-active buffer. The basic concept for the depth marker feature is that once the programmed depth (i.e., display scan line) has been reached, no other memory sources (i.e., video input update scan line) can overlap the previously marked resource and causes undesirable visual effects. Registers 68h defines the Video Input Update Depth Marker. Registers 8Ah define the capture depth marker. Register 93h defines the display depth marker. In dual buffer mode the setting of these registers is critical to the function of the VxP202. In quad buffer mode the setting of the buffer depth registers is not as critical because deadlock is not possible. The correct depth must be determined which guarantees that the write pointer (input) will not be overtaken by the read pointer (output) without locking the buffer too much and thereby deadlocking the system and forcing frames to be dropped. In order for dual buffer to operate correctly, it can be shown that the combined input and output locking time must be less than 100% for not frame dropping to occur. It can also be shown that when both the input and the output are progressive scan then the aforementioned requirement can be met. In the case of interlace sources, each field should be treated as an independent frame. For example the input should treat each field as an independent frame and zoom out by 2 vertically for a full frame. The output also treats each field as a new frame of half the size. Normally software playback and motion capture will use quad buffer mode. Only full frame or larger live video is forced to use dual buffer. It is in this mode that the buffer depths must be determined. The line rate for the input and the output must be determined. In the case of the input this can be calculated depending on whether the input is NTSC, PAL, custom (sync gen.), etc. The output needs to be determined from the output clock and the graphic buffer resolution. The line rate is calculated with respect to the buffer. So if for example the input is being scaled by 1/2 then the line rate is reduced by 1/2 etc. Likewise with the output, if the video is being zoomed vertically by 2 then the line rate is reduce by 1/2. Once the line rates are determined then the buffer depths can be set. To set the input depth, first determine if the input or output rate is faster. If the input is faster than the output then presumably, the output cannot pass the input pointer and the buffer can be released almost immediately. Possibly a 1 or 2 line buffer should be left to account for synchronization between the pipelines. If the output is faster than the input, then the depth at which the input can release the buffer which guarantees the output won't overtake it needs to be determined. The same process is used to determine the output buffer depth. The capture buffer depth is usually set to the last line, because the ISA transfer rate is indeterminate and capture is usually done in quad buffer mode. The exception to this is hardware capture, because the capture rate can be determined.

Input Filter Definition:

50h Input Filtering Register

The VxP202 input pipeline supports the two dimensional luma and chroma filters. Horizontal filtering can be performed on both luminance and chrominance data. Vertical filtering is performed on luminace data only.

Horizontal luma filtering can be one of four selections, no filter, 2, 3, or 4 taps FIR filter (bits 1-0, 50h). The horizontal chroma filter is a two tap FIR filter that operates in two modes , no filtering or 2 tap filter (bit 2 , 50h).

The vertical luma filter is also a two tap FIR filter that operates in 2 modes, no filtering or 2 tap filter. When the vertical filter control bit is set (bit 4, 50h), then two tap filter operation is performed, and the line buffer for the input pipeline is enable for vertical interpolation. In this mode, all video data are the average of two lines (except the first line). For interlace video, each line will be the average of two even or two odd lines.

Rgister 50h provides the filtering control function. Bits (4-0) of this register selects the filter mode for horizontal and vertical filtering. Bits 6 and 7 of this register provide the selections for drop or overwrite mode and uniform or paired mode for vertical scaling.

54h,55h,5Bh,5Ch,6Dh,50h Horizontal, Vertical and Time Scaling Control Registers

VxP202 uses a carry accumulate algorithm for scaling controls. Horizontal scaling is done by dropping pixels. Vertical scaling can be done by dropping or overwriting the lines in either uniform or paired mode . The Horizontal and Vertical scaler each contain a 10 bit scaling value and the time scaler contains an 8 bit scaling value. The 10 bit scaling value allows a scaling ratio from 1 in 1024 to 1023 in 1024. The Horizontal, Vertical and Time Scaling Control registers control the scaling functions. The carry accumulate algorithm functions as follow: The programmed number accumulates (adds to itself) on every valid pixel, line or frame. A line, pixel or frame is kept (scaled) if a carry is generated from the previous accumulation (adding).

For example.

A. 00 0000 0000b in the horizontal scaling register means no scaling, since adding 0 to itself will never generate a carry.

B. 10 0000 0000b means scale to 1/2 (drop every other pixel), since 200h will generate a carry every other additions.

C. 01 0000 0000b means scale to 1/4, since 100h will generate a carry every fourth addition.

D. 11 0000 0000b means scale to 3/4, since 300h will generate a carry three out of four additions.

VxP202 offers two types of vertical scaling. They are paired and uniform scaling (See figure 3.2.1).

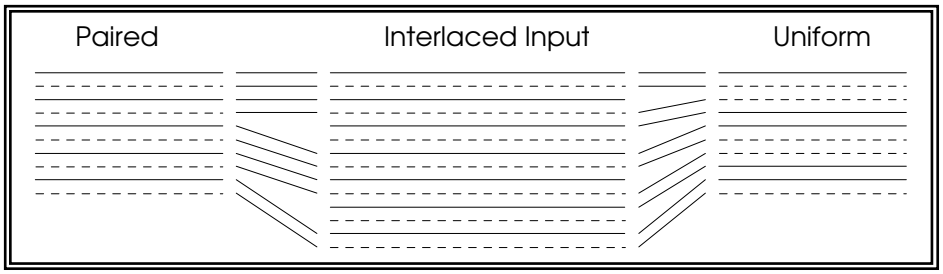


Figure 3.2.1

Paired scaling are designed for interlaced motion video (note: not recommended with overwrite mode on). By dropping video lines in odd and even pairs, motion artifacts are more difficult to detect under normal conditions. Since a fast moving image occupies two different screen positions between the even and odd frame of video data, an image can have a finite offset between the even frame and odd frame. If vertical scaling is not done in pairs, the same image that lies on the even and odd fields, in addition to having a offset, can also have different shapes. Under this condition, the motion artifact can be detected (even at 60 frames per second). With VxP202 live video never uses interlace mode, uniform or paired scaling is not an issue. It is only necessary for capturing full resolution still images.

The uniform vertical scaling will provide a smoother line to line transition since it drops fewer lines between active scan line, especially when the image contains a diagonal line with a small horizontal angle. Bit (7) of the Filter Control register (50h) selects the mode for paired or uniform vertical scaling. Uniform scaling however causes more distacting motion artifacts than the paired scaling algorithm.

Overwrite Mode:

VxP202's overwrite mode controls whether lines are dropped or written over previous lines. In drop mode lines that are removed due to scaling are not written to memory. In overwrite mode lines that are removed due to scaling are written over the previously written line. For motion video this has the effect of removing motion artifacts when less than half screen. In the VxP202 however live video is always done in progressive mode so this should be set to drop mode.

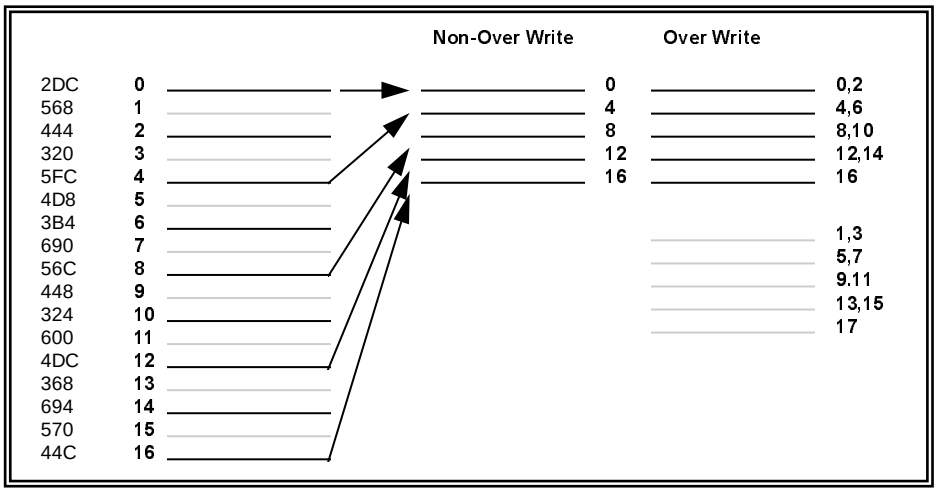


Figure 3.2.2 Overwrite On verse Overwrite Off in Space domain

Register 54h and 55h provide the horizontal scaling control values, registers 5Bh and 5Ch provide the vertical scaling control values. To select overwrite mode, set the VD_O bit (6) of the Filter Control register (50h) to "1", otherwise drop mode will be selected.

VxP202 also supports time scaling as a solution for video synchronization during periods when full frame rate can not be supported due to bandwidth and system restriction. Time scaling function drops frames to provide this solution. Register 6Dh provides the time scaling factor. When this register is zero then all fields are captured, any other number represents the number of fields to capture for every 256 fields that enter.

Note: When the capture frame rate is less than the incoming video frame rate and the continuous capture mode is used, time scaling will be necessary. For example: If the income video is 60 fps, time scaling is required if the hardware can not also support 60 fps capture. In a multi-buffer configurated system, video frames will be dropped if the capture buffer is not ready by the time input buffers are full. Video frames dropped in this way instead of using the time scaling function will have poor frame distribution (more time jitters).

40h,41h,44h,45h,48h,49h,4Ch,4Dh, Horizontal, Vertical Cropping Registers

VxP202 crops the incoming video before it is scaled (see figure 3.2.0). The four sets of cropping registers, left, right, top and bottom crops the four respected edges of the incoming video. Each unit specifies one scan line or one pixel. For decoded video, vertical and horizontal SYNC are used as reference. For ISA bus playback the ISA source width and height are used. The left and top cropping boundary values will be the same as the values specified by the horizontal cropping left (40h, 41h) and verical cropping top registers (48h, 49h). The right and bottom

cropping boundary values will be one pixel or scan line less than the values specified in the horizontal cropping right (44h, 45h) and vertical cropping bottom (4Ch, 4Dh).

78h Input FIFO

This register specifies the low and high markers for the input pipeline FIFO. See the general section for an explanation on how to set this register.

60h, 61h Video Input/Capture Interrupt Control and Status Registers

VxP202 can be programmed to generate eight input and capture interrupts. They are as follow:

1. Input Even Field (bit 0, 60h): If enabled (set to "1"), an interrupt is generated whe never VxP202 is processing the even field of an interlaced input video.

2. Input Odd Field (bit 1, 60h): If enabled (set to "1"), an interrupt is generated whenever VxP202 is processing the odd field of an interlaced input video.

3. Acquiring New Frame (bit 2, 60h): If set, an interrupt is generated whenever VxP202 begins to acquire a new frame of video data.

4. Video In Enabled (bit 3, 60h): If set, an interrupt is generated whenever VxP202 begins accepting video data from the video input bus. Note: video source is selected by the input video configuration registers (38h & 39h). The selection may not actually take place until the end of a video frame. Refer to the video configuration register description in this document for additional details.

5. Capture FIFO contains data: (bit 4, 60h): if set, an interrupt is generated whenever the captured data is ready at the end of the capture pipeline.

6. FIFO data drop: (bit 5, 60h): If set, an interrupt is generated whenever input data is dropped due to i nsufficient bandwidth to the memory controller.

7. DMA TC (bit 6, 60h): If set, an interrupt is generated whenever the VxP202 has successfully completed a DMA transfer.

8. Video In disable (bit 7, 60h): If set, an interrupt is generated whenever the VxP202 video input decoder is turned off. This may not take place until the end of a video frame.

There are also interrupt status bits for each of the foregoing interrupt conditions. These bits are in the Video Input Interrupt Status register (61h) and are set when the corresponding interrupt conditions are met and are cleared by writing ’0’ to each bit.

3.3 Video_Out Register

Output Pipeline Control & Status Registers

Index	Register Name
90h	Output Pixel Buffer Low & High Mark
92h	Display Control
93h	Output Frame Buffer (Multi-Buffer) Depth Control
94h - 95h	VGA Control & B
96h - 98h	Output Processing Control A & B & C
9Ah	Palette Read Address High Nibble
9Bh	Chroma Key Control (Delay)
9Ch	Key Color
9Dh	Key Color High (Byte 1)
9Eh	Key Color High (Byte 2)
A0h	Display View Port Starting Address A
A4h	Display View Port Width A
A6h	Display View Port Height A
A7h	Display View Port Starting Address/Width/Height B
A8h	Display View Port Display Origin Top A
AAh	Display View Port Display Origin Left A
ABh	Display View Port Display Origin Top/Left B
B0h	Display Window Left A
B4h	Display Window Right A
B5h	Display Window Left/Right B
B8h	Display Window Top A
BCh	Display Window Bottom A
BDh	Display Window Top/Bottom B

Table 3.3.0

Index	Register Name
C0h - C1h	Output Vertical Zoom Control A & B
C4h - C5h	Output Horizontal Zoom Control A & B
C6h	Vertical Coordinate Offset
C7h	Horizontal Coordinate Offset
CBh - CCh	GPO Data 0 & 1
CDh - CEh	VGA Control C & D
D0h - D1h	Max Hcount 1 & 2
D2h	Video Output Interrupt Control
D3h	Video Output Interrupt Status
D5h - D7h	VGA Data Byte 0 & 1 & 2
D8h - D9h	Chroma Key Red Low & High
DAh - DBh	Chroma Key Green Low & High
DCh - DDh	Chroma Key Blue Low & High

Table 3.3.1

Display view port addresses, window, key colors and chroma key definition:

VxP202's display output is controlled by eight parameters: video frame buffer start address, display view port origin, width, height, color key, display window, chroma key and VGA data. These display parameters control the placement and display condition of video and VGA data on the RGB monitor (See Figure 3.3.0 and 3.3.1).

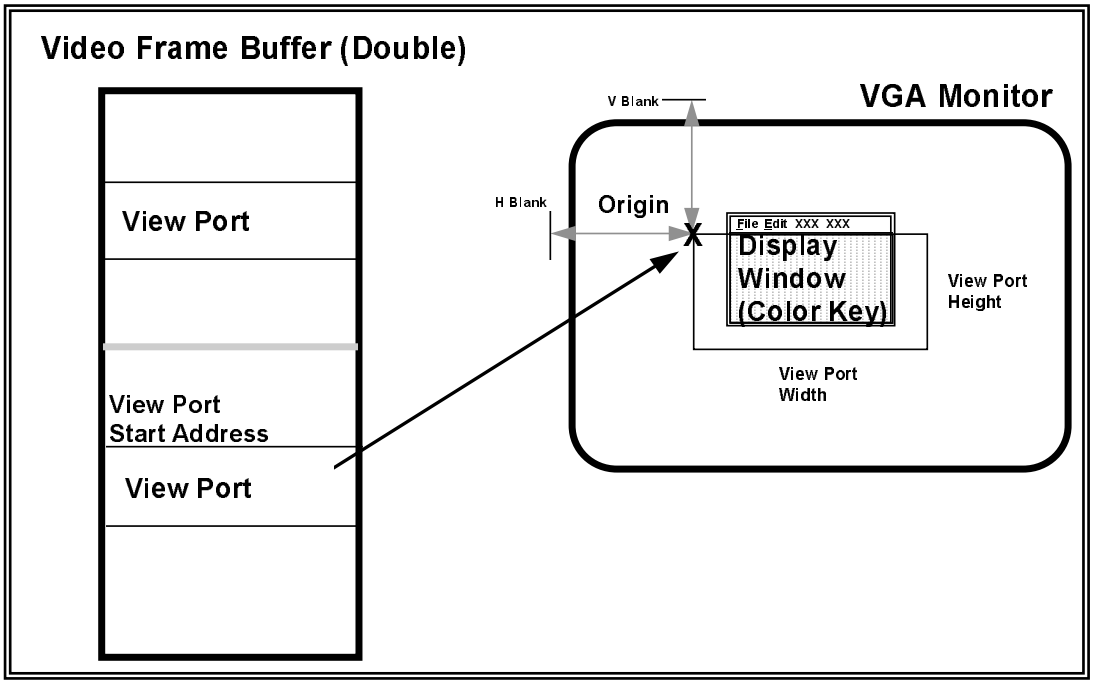


Figure 3.3.0 Display Conceptual Diagram

A0h,A7h,A8h,AAh,ABh Display View Port Starting Address and Screen Origin

VxP202's display view port's size and location can be independent from acquisition and capture window. The view port starting line number (pseudo-address) and screen origin both point to the upper left hand corner of the display view port. The starting line specifies the view port vertical coordinate in the video frame buffer. The view port screen origin specifies the upper left hand corner of the view port relative to the VGA Horizontal and Vertical Blank. The origin top parameter defines the upper left hand corner relative to the VGA vertical Blank (a little above the visible top of screen) and the value must be 3 or larger because the videoout pipeline begins requests to memory controller only when the VGA line count has reached a value two smaller than the origin top value. The origin left specifies the same corner relative to the VGA horizontal Blank (a bit to the left of the visible screen) and must be 5 or larger to ensure the VGA coordinate state machine delay has been met. If software wants to display the same video data that is being acquired, the display frame buffer line value should be zero as all acquisition frames have offsets of zero within each frame. Non-zero view port starting line provides a video frame with the top portion clipped. By changing the display origin coordinates, software can place the acquired video anywhere within the VGA screen. Note: Video data are not displayed unless the view port also falls within a display window and both the color and chroma keys match.

A4h, A6h, A7h Display View Port Height and Width

If software wants to display the same video data that is being acquired, the display view port starting line value should be zero and the width and height of the display view port should be the same as the final video input size (cropped and scaled). Note: video data are not displayed unless the view port also falls within a display window and both the color and chroma keys match.

Example: if Input video = 720 by 480
20 lines cropped on both top and bottom
10 pixels cropped on both left and right side
Scaled = 1/2 vertical and horizontal
Memory Interleave factor = 2
VGA monitor = 640 by 480
Display View Port Origin = line #25 (actual 26th line from top)
Display Window location = 40 lines from the V Blank and 50 pixels from the H Blank

Then Display, Capture and line value = 25
Capture Window Width = ((720 - 10 - 10) / 2)/2 = 175
Capture Window Height = (480 - 20 - 20) / 2 = 220
Display View Port Width = ((720 - 10 - 10) / 2)/2 = 175
Display View Port Heigth = (480 - 20 - 20) / 2 - 25 = 195
Display Window Origin Top = 40
Display Window Origin Left = 50

Combining Video and VGA data:

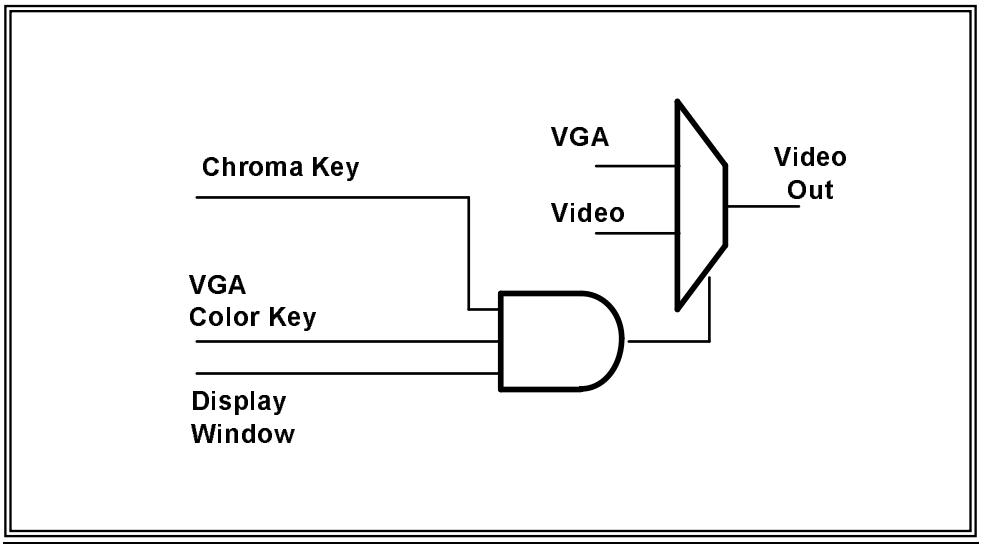


Figure 3.3.1 Conceptual Diagram Video/VGA Multiplexing

Figure 3.3.1 illustrates the output display selection process between the video in the display view port and VGA data.

1. View Port must fall within display window (This function may be turned off)
2. View Port must overlay on color key that is specified by the key color register
3. Video data must overlay on colors that match the programmed chroma range (skip if chroma key is disabled).

Refer to the display control register (92h) descriptions for additional display control details.

B0h,B4h,B5h,B8h,BCh,BDh Display Window left, right, top and bottom

These register specify the size and location of the display window. If software wants to display the same video data that is being acquired, the display view port should be zero and the width and height of the display view port should

be the same as the final video input size (cropped and scaled). In addition, the display window size and location must match the display view port. See fig 7.0.

Example: if Input video = 360 by 240
20 lines cropped on both top and bottom
10 pixels cropped on both left and right side
Scaled = 1/2 vertical and horizontal
Zoomed = 1.5 vertical and horizontal
Memory Interleave factor = 2
VGA monitor = 640 by 480
Display Window location = 40 lines from V Blank and 50 pixels left of H Blank.

Then Capture Window Width = (360 - 10 - 10) / (2 * 2) = 85
Capture Window Height = (240 - 20 - 20) / 2 = 100
Display View Port Width = (360 - 10 - 10) / (2 * 2) = 85
Display View Port Height = (240 - 20 - 20) / 2 = 100
Display Window left , top = 50 , 40
Display Window right = 50 + (85 * 2 * 1.5) = 305
Display Window bottom = 40 + (100 * 1.5) = 190

View Port and Display Window Restrictions:

Unlike the VxP500 which requires that the display view port not overlap into the blanking areas on the right of the VGA screen, VxP202 allows these conditions. The change allows display view port wraparound which is required if the display view port is to visually wrap into the left of the VGA screen. In Fig 9.0, the display viewport origin may be placed anywhere in the VGA coordinate screen with either color key and/or display window values set to display only one section of the viewport display window. However, while the left drawing on Fig 9.0 is allowed, it is recommended that any video which would reside beyond the right blank portion should be cropped appropriately to save memory bandwidth.

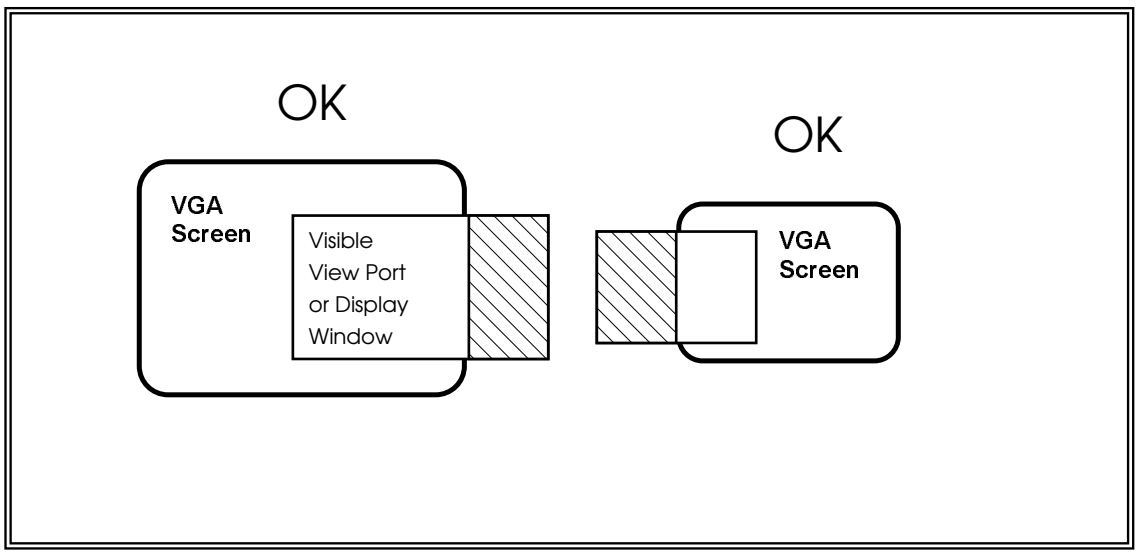


Figure 3.3.2 Display View Port and Window

9Ch,9Dh,9Eh Key Color Registers

The key color registers specify the VGA color key. Register 9Eh is the most significant byte. It is only used with 24 bit VGA where the color key is 24 bits wide. Register 9Ch is used with in 8 bit VGA mode, 9Ch and 9Dh in 16 bit

VGA mode, and 9Ch, 9Dh, and 9Dh in 24 bit VGA mode. Note that in high-speed-bypass mode, all bytes are compared to only 9Ch (8 bit compare only). It is also possible to turn off color key matching altogether, in which case a color key match is always generated. See display control register description, 92h.

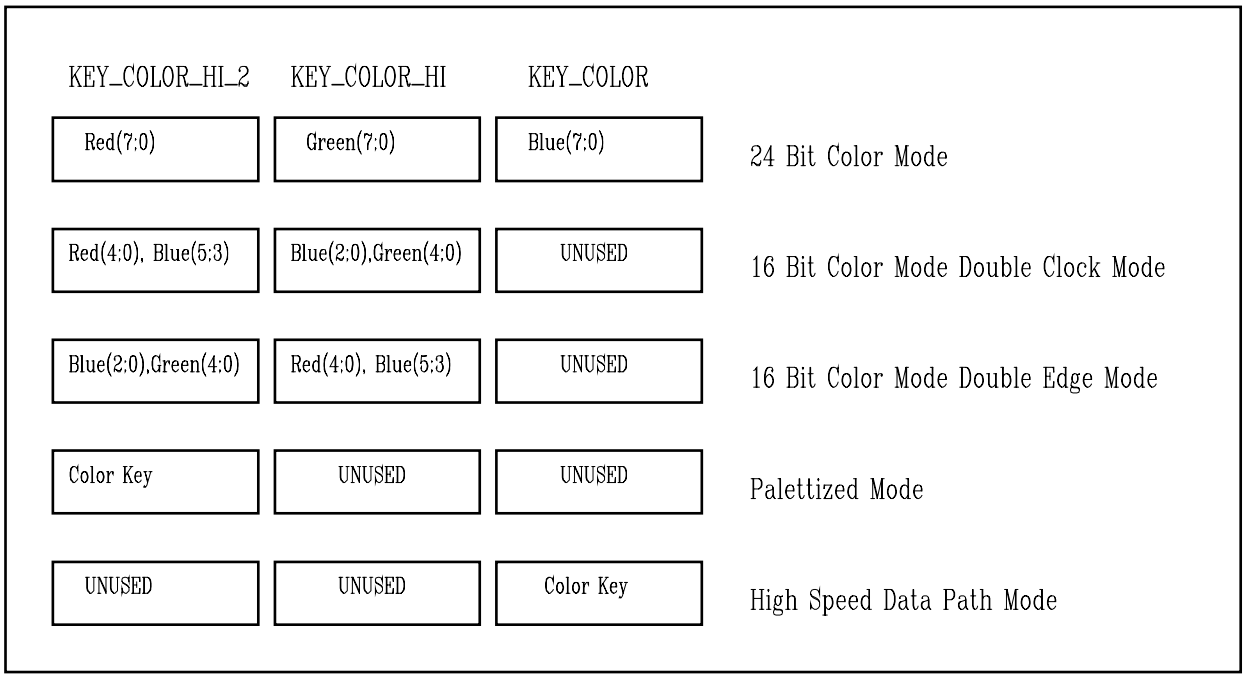


Figure 3.3.3Display View Port and Window

Chroma Key Registers

D8h,D9h,DAh,DBh,DCh,DDh Chroma Key Registers

In addition to supporting color key, VxP202 also supports chroma key. A color key allows video to overlay onto VGA graphics based on the color of the VGA data. The chroma key also allows the overlay of video on top of VGA graphics. However, the overlay is based on the video chroma data rather than VGA color data. An example of this is in TV news broadcasts where the weather man (video) moves around in front of a weather map (graphic). The following example illustrates how this task may be accomplish using the VxP202:

Example: A weather man (video) moves around in front of a weather map (graphic)

Assume: The video consists of a weather man moving around in front of a blue back ground. Blue was selected because its chroma value is all blue and contains little or no red or green color. This simplifies the chroma key programming process. Note: If blue is selected, the weather man is not allowed to wear blue or else the weather map will overlay on top of his blue garment. VxP202 allows any number of chroma values for chroma keys.

Next: Program the estimated chroma value of the background color into the chroma ke y registers (see figure 3.3.3). The registers only take a 6 bit value which is then multiplied by 4 to perform the chroma comparison.

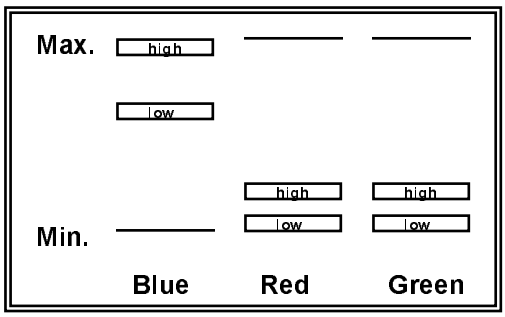


Figure 3.3.4 Chroma Keys for a Blue Background

92h Display Control Register

This register contains eight fields, VGA color key enable (VKE), VGA 16 bit direct color key enable (VDCE), VGA display window enable (VDWE), video output region select (ORS) and high speed video selection bits. Together, they define the video display selection criteria (see table 3.3.2). The remaining three fields provide analogous control for the windowing, color keying, and chroma keying in high-speed-bypass mode.

VGA color key enable (VKE)	VGA 16 bit-555 Color Key Enable (VDCE)	VGA display window enable (VDWE)	video output region select (ORS)	Display Select Match Criteria
0	X	0	XX	View Port Only
0	X	1	0X	View Port & Display Window
1	0	0	X0	View Port & Reg Color Key
1	0	0	X0	View Port
1	1	0	X0	View Port & 16 bit 555 Key
1	0	1	00	View Port & Reg Color Key & Display Window
1	0	1	00	View Port & Display Window
1	1	1	00	View Port & 16 bit 555 Key & Display Window
X	X	X	11	View Port Only
Note: All other combinations are not allowed. Chroma key is controlled by the Chroma Key Enable (CKE) bit in the Output Processing Control A register (96h).				

Table 3.3.2 Display Select Match Criteria

VGA color key enable (VKE)	VGA 16 bit-555 Color Key Enable (VDCE)	VGA display window enable (VDWE)	video output region select (ORS)	Display Select Match Criteria
0	X	0	XX	View Port Only
0	X	1	0X	View Port & Display Window
1	0	0	X0	View Port & Color Key
1	0	0	X0	View Port & Color Key & Display Window
1	1	0	X0	View Port & 16 bit 555 Key
1	0	1	00	View Port & Reg Color Key & Display Window
1	0	1	00	View Port & Display Window
1	1	1	00	View Port & 16 bit 555 Key & Display Window

X	X	X	11	View Port Only

Table 3.3.3 Display Select Match Criteria in High Speed Mode

94h VGA Control Register

The VGA control register selects the VGA system that VxP202 interfaces to.

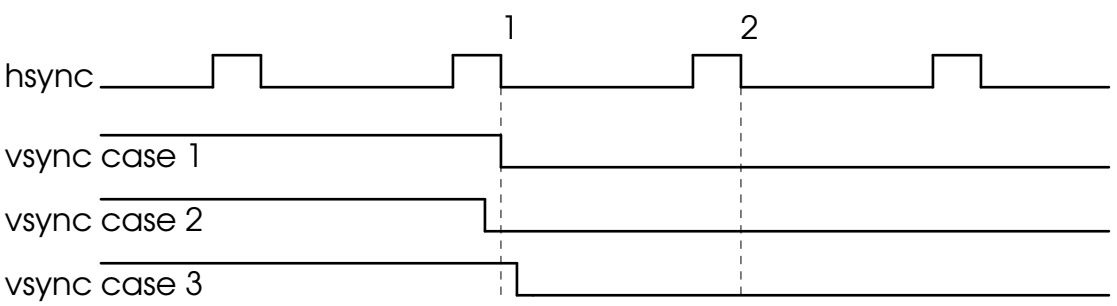
VGA direct color 16 enable (DC16E)	VGA direct color double clock (DCDC)	24 bit direct color (DC24)	high speed data path enble (HSCSEN)	high speed video clock select (HSCS)	advanced feature connector enable (AFCE)	advanced feature connector extended mode (AFCEME)	VGA TYPE
0	X	0	0	XX	0	X	Palettized
1	0	0	0	XX	0	X	16 bit color 2 clocks/pixel (double clock)
1	1	0	0	XX	0	X	16 bit color 1 clock/pixel (rising/falling edge)
0	0	1	0	XX	0	X	24 bit color
X	X	X	1	01	0	X	80 MHz < VGA clock < 90 MHz
X	X	X	1	10	0	X	90 MHz < VGA clock < 135 MHz
X	X	X	1	11	0	X	135 MHz < VGA clock < 180 MHz
X	X	X	0	XX	1	0	advanced feature connector mode
X	X	X	0	XX	1	1	advanced feature connector mode (extended)

Figure 3.3.5 VGA Input Setup

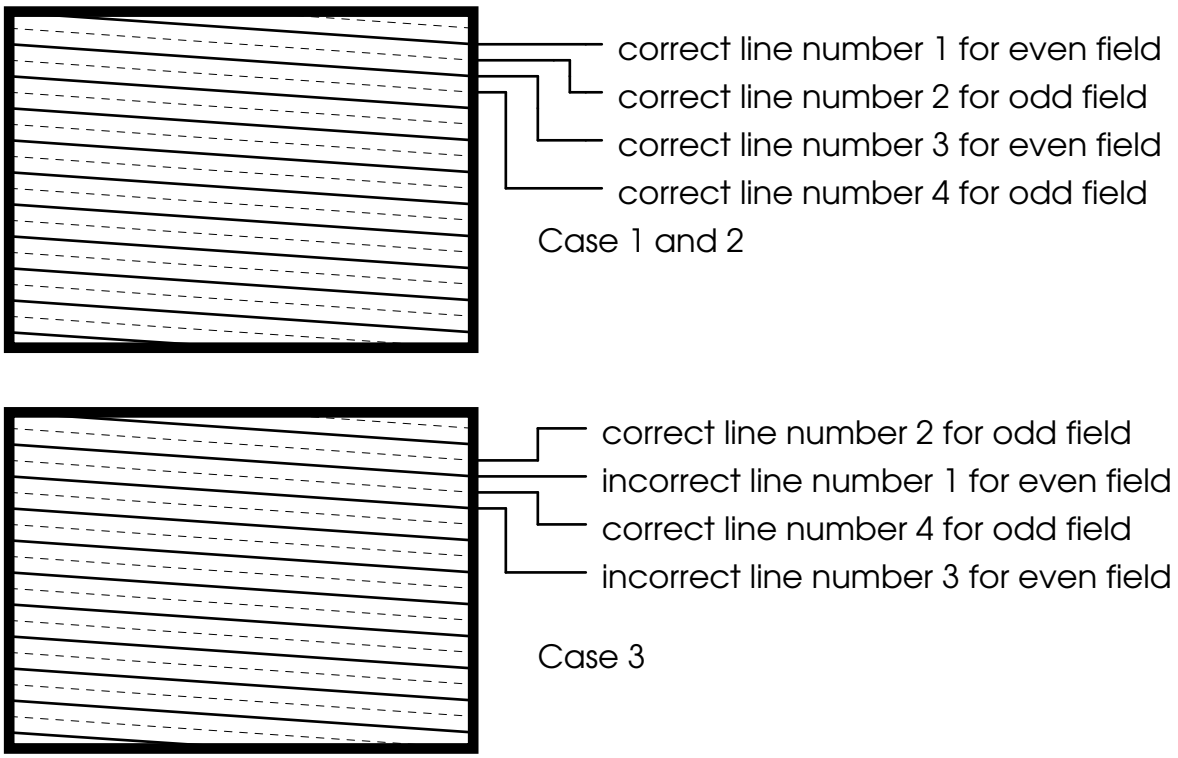
94h, 95h VGA Control Register (continue)

Interlaced software interaction:

If VGA is in interlaced mode (bit 0 of VGA Control, 94h), there are two bits within the VGA Control B register which software can use to ensure correct internal counting of even field lines.

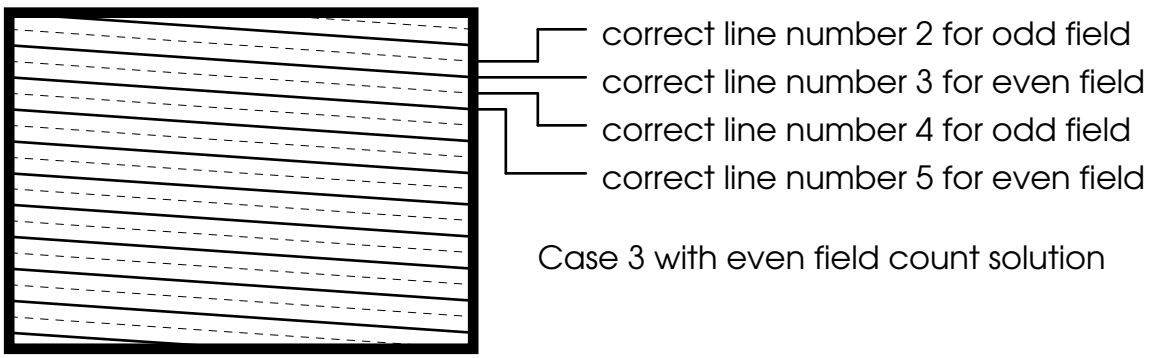


The hzoomer block begins counting field lines at the first hsync deactivation edge where vsync has deactivated. Therefore, in the above figure, which represent the start of an even field, case 1 and 2 will begin the internal line count at location 1, while in case 3, because the vsync deactivation was not yet visible at hsync deactivation point 1, the internal line count will not start until location 2. Thus, in case 3, which was a case seen in the lab using the Spider VGA card, the even field count would be off by 2 (interlace mode increment line count by twos) leading to a tearing effect of the even and odd field.



VGA screen in interlaced mode

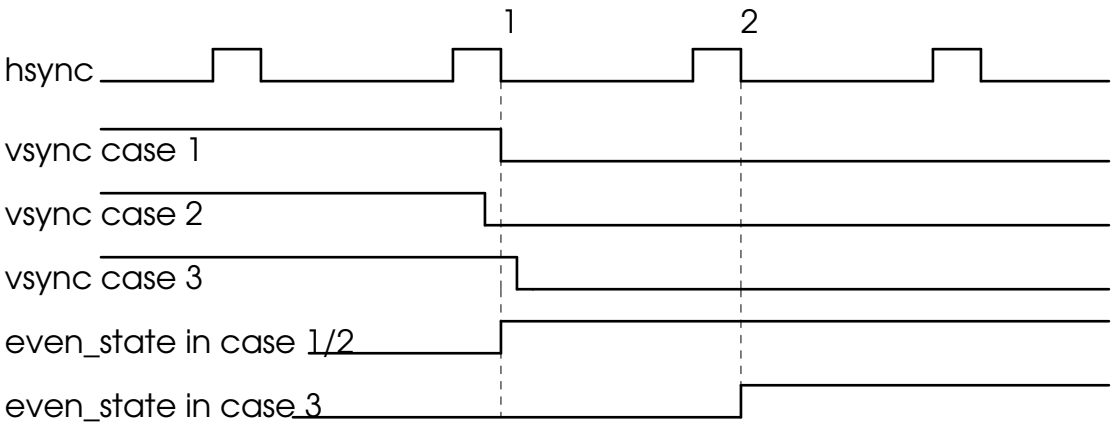
As stated before, two bits were added to the VGA CONTROL B register to provide a solution to this problem of miscounting even field lines when the VGA is in interlaced mode. Bit 1 of this register is EVEN_INC. This bit, when set, will start even field counts at 3, otherwise it will start with 1. Now, all software needs is a method to discover when the VGA sync timing correspond to case 1 / 2, or to case 3. Obviously, in case 1 / 2, the EVEN_INC bit will be set to zero and in case 3, it will be set to one.



VGA screen in interlaced mode

To find which case is occuring, software must read the EVEN_STATE (bit 2 in VGA CONTROL B register) value after time location 1 (see below). Software should already know whether the VGA is in even field or odd field

(using the VGA_DATA register to read a written pixel from an even field line). When approaching the start of an even field, software would read the EVEN_STATE bit at a time between location 1 and 2. If it is high, software should set the EVEN_INC bit to zero, and if EVEN_STATE is low, EVEN_INC should be set to one.



96h,97h,98h Output Processing Control Registers

565 output enable (565EN)	internal muxing enable (IMUXEN)	VGA output data mux enable (MUXEN)	VGA output data mux mode (MUXMODE)	VGA synchronous output delay (SDLYEN)	VIDEON enable (VIDNEN)	OUTPUT TYPE
0	1	0	0	1	0	SGS ? with digital muxing (16 bit or 24 bit color only)
0	0	0	0	1	1	SGS ? with analog muxing
1	1	0	0	1	1*	ATT 498 RAMDAC with digital muxing
1	0	0	0	1	1	ATT 498 RAMDAC with analog muxing
0	1	1	1	1	0	ATT 489 RAMDAC with digital muxing (16 bit or 24 bit color only)
0	0	1	1	1	1	ATT 489 RAMDAC with analog muxing

* should be 0 if VGA input is not palettized data

Figure 3.3.6 Output Setup

Horizontal Zoom Enable, Interpolation bits (HZME, bit 1, HIE, bit 2, 96h):
Horizontal zooming is enabled the moment this bit is set. Interpolation will only become evident when horizontal zooming is enabled. Interpolation occurs up to 4X zoom after which, replication occurs.

Chroma Interpolation Enable (CIE, bit 5, 96h):
When video data is YUV422, every other chroma data is interpolated from its two chroma neighbors. YUV411 chroma is interpolated for 3 of the 4 pixels in each 411 chroma block.

Vertical Zoom Enable bit (VZME, bit 0, 97h):
Once this bit has been enabled, and the viewport control register load enable bit is toggled high, the videoout pipeline will be in vertical zoom mode on the next frame read from the frame buffer.

Vertical Interpolation Enable bit (VIE, bit 1, 97h):
Once this bit is set and vertical zooming is already enabled, the videoout pipeline will be immediately in vertical interpolation mode.

Video Output Enable bit (VOUT_EN, bit 5, 97h):
Setting this bit allocates pixel cache resources to the display and enables the display pipeline. Note: software must insure that the VxP202 is in the global reset state before changing this bit.

Video Output Reset (VOUT_RESET, bit 6, 97h):
The Video Output Reset bit, if set, places the output display pipeline at its reset state.

View port Control Register Load Enable (RLE, bit 7, 97h):
The View port Control Register Load Enable bit (RLE, bit 7, 97h) is used to synchronize view port controls. This allows the update of view port control registers while the display output pipeline is processing active video data. The RLE field controls the following view port control signals:

1. Video Buffer Layout Control Register (73h)
2. VGA Interlace Output (INLC, bit 0, VGA Control register, 94h)
3. Memory Mode (MM, Memory Configuration Register, 18h)
4. Display View Port Start Address Registers (A0h,A1h,A2h)
5. Display View Port Width/Height Registers (A4h,A5h,A6h,A7h)
6. V Zoom Enable (Output Processing Control A register, 96h)
7. Output Vertical Zoom Control Registers (C0,C1h).

When changing the control parameters listed above, software should clear (set to "0") the View port Control Register Load Enable bit (RLE) before changing any parameters. When all the view port control parameters are changed, the RLE bit should then be set (to "1"). VxP202 will wait for the end of the current view port data transfer before it applies the changes to the display output pipeline.

The following controls are also provided by the Output Processing Control registers:

1. Horizontal Zoom Enable (bit 1, 96h active 1)
2. Horizontal Interpolation Enable (bit 2, 96h active 1)
3. Chroma Interpolation Enable (bit 5, 96h active 1)
4. Chroma Key Enable (bit 6, 96h active 1)
5. Vertical Zoom Enable (bit 0, 97h active 1)
6. Vertical Interpolation Enable (bit 1, 97h active 1)

9Ah Palette Read Address High Nibble Register

The VxP202 does not contain a palette, but it can be used to control the palette on ATT498 RAMDAC.

This register contain two fields, High Order Palette Address (PA, bit 3:0) and Palette Read Enable (PRE, bit 7). The PRE field specifies the 4 most significant bits of the ATT498 color palette I/O address. These bits are defaulted to 0 at hardware reset and allow the ATT498's color palette to occupy the standard VGA color palette address space at power up. Changing the PA field relocates ATT498's color palette to other I/O locations.

The Palette Read Enable (PRE) controls the read function of the ATT498 color palette. In a system where the VGA contains its own color palette (i.e., a system that relies on the VGA feature connector), ATT498's color palette should be slaved to the VGA palette. ATT498's color palette should responds to ISA bus write access only. In this configuration, ATT498's color palette is always a duplicate copy of the VGA color palette. By not responding to ISA read access, any possibility of data contention is avoided. In a system where ATT498's color palette is the only color palette in the system (i.e., a combined VGA/Video system), ATT498's color palette should respond to both ISA read and write access. The PRE bit defaults to "0" (not enabled) at hardware reset.

Note: The power configuration register (11h) also contains a color palette enable bit. ATT498’s color palette is controlled by the logical "OR" function of the two color palette enable bits (see table 3.3.4).

Power Up Config. (11h) Palette Enable	Palette Address Reg. (9Ah) Palette Enable	
0	0	ATT498's color palette responds to ISA write access only. This is the normal configuration, if there are two color palette in the system.
0	1	ATT498's color palette responds to ISA read and write access.
1	X	ATT498's color palette responds to ISA read and write access. This is the normal configuration, if ATT498's color palette is the only color palette in the system

Table 3.3.4

C0h,C1h,C4h,C5h Output Vertical/Horizontal Zoom Control

Similar to scaling, VxP202 uses a carry accumulate algorithm for zoom controls. The Horizontal and Vertical zoomer each contain an 11 bit zoom value. The 11 bit scaling value allows a zoom ratio from 1 in 2048. The Horizontal, and Vertical Zoom Control registers control the zoom functions. The carry accumulate algorithm functions as follows: The programmed number accumulates (adds to itself) on every valid pixel or line. A new line or pixel is output (displayed) if a carry is generated from the previous accumulation (adding). For cases where no carry is generated, the displayed pixel is the linear interpolation of two pixels (one in front and one behind). VxP202 can perform interpolated horizontal and vertical zoom up to 4X. For zoom factor that is more than 4X, the remaining zoom will be completed without any interpolation.

For example.

A. 000 0000 0000b in the horizontal zoom register means no zooming, since adding 0 to itself will never generate a carry. Zoom factor = 1 + 0.

B. 100 0000 0000b means zoom to 2X (duplicate every other pixel), since 400h will generate a carry every other addition. Zoom factor = 1 + 1.

C. 010 0000 0000b means zoom to 4X, since 200h will generate a carry every fourth addition. Zoom factor = 1 + 3.

D. 110 0000 0000b means zoom to 1.25X, since 600h will generate a carry three out of four additions. Zoom factor = 1 + .25.

Note: ATT498 zooms from the upper left hand corner of the display window. See figure 3.3.7.

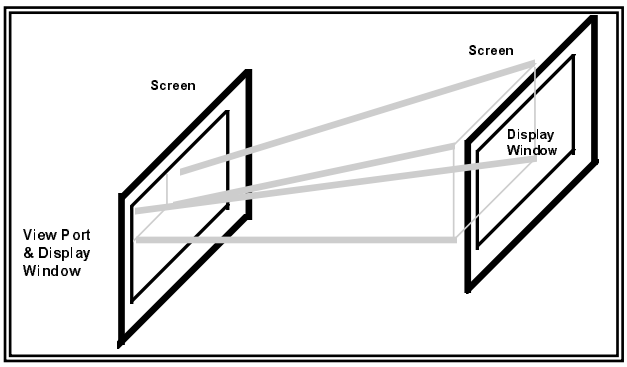


Figure 3.3.7 VxP202 Zoom

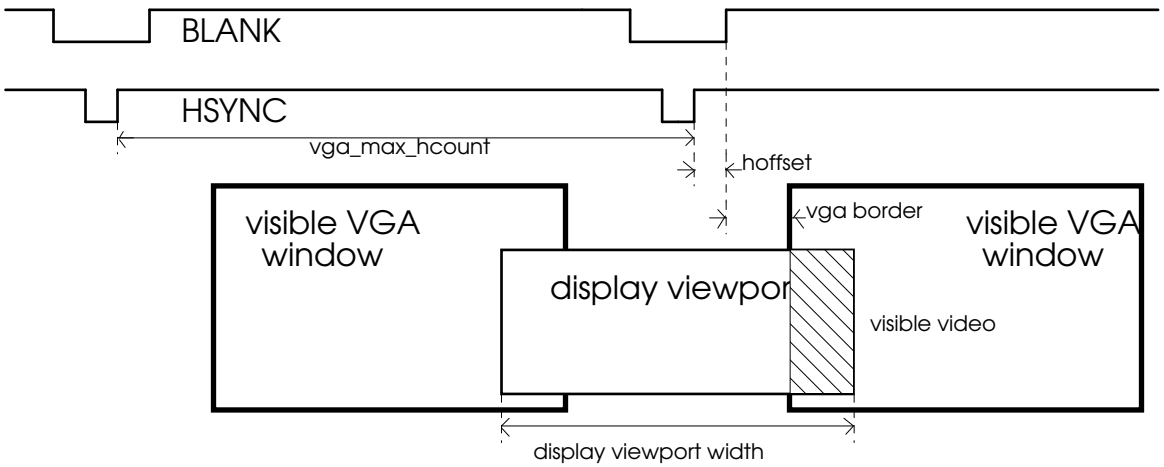


Figure 3.3.8 Display Viewport Origin Left

C6h,C7h,D0h,D1h Vertical and Horizontal Offset Registers, Max Hcount Registers

See Fig 13.0. The vertical and horizontal offset registers provide the number of VGA pixels between the end of vsync and hsync respectively to the origin of the visible VGA window. These values are used to calculate the display viewport window and origin values. There is also the VGA max hcount register which allows software to read the maximum number of horizontal pixels in one VGA line. Along with the VGA border value (which software can find with read/writes to VGA memory) and display viewport width (with hzoom = viewport-width register value * memory interleave * 2048 / hzoom control value), software can now easily calculate the display origin left value required when wrapping the visible video into the right boundary of the VGA window.

disp vp origin left = vga_max_hcount - (disp vp width - hoffset - vga border width) + # visible video pixels

CDh VGA Control C

Some VGA cards may require clock compensation. Some may produce a VGA clock which may have a very unsymetric duty cycle. If this is the case and the VxP202 appears as though it is not receiving a clock, then it may be necessary to adjust with VGA_CONTROL_C(0) and VGA_CONTROL_C(6:5). Set VGA_CONTROL_C(6:5) = ’11’. VGA_CONTROL_C(0) can then be used to select the type of compensation. When VGA_CONTROL_C(0) = 0 the low portion of the cycle is extended. When VGA_CONTROL_C(0) = 1 the high portion of the cycle is extended. See Figure 3.3.9.

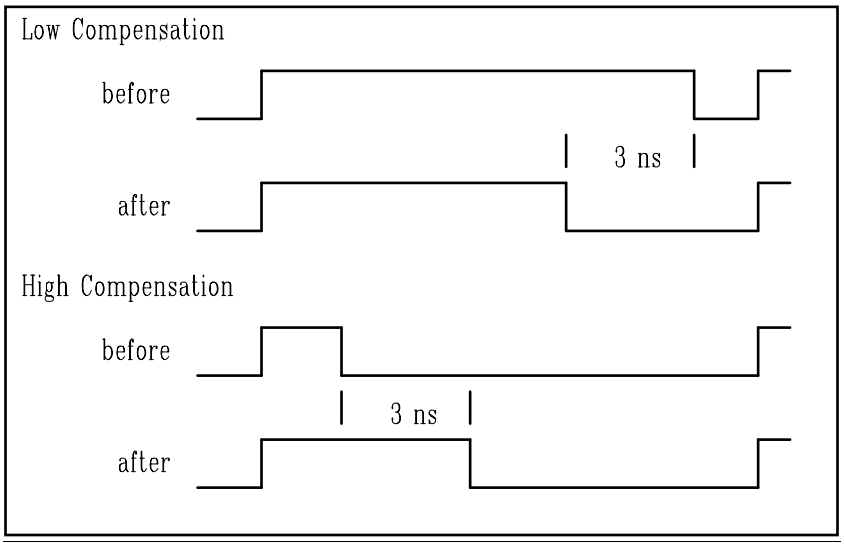


Figure3.3.9 Clock Width Compensation

With some VGA cards it may be necessary to skew the clock/data timing to compensate for feature connector timing skew. If digital muxing is used the problem may show up as either incorrect VGA coloring or colored snow in the VGA or video region. If analog muxing is used then there may be colored snow in the video region.

The problem can be reduced by varying the clock/data timing with VGA_CONTROL_C(4:1). The timing can be changed open loop or closed loop as described below.

Open Loop - Set VGA_CONTROL_C(4:1) = ’111’ then decrease the value until the coloring is correct.

Closed Loop - Set VGA_CONTROL_C(4:1) = ’111’ then read back the VGA data which is latched by VGA_DATA_BYTE_0, VGA_DATA_BYTE_1, and VGA_DATA_BYTE_2. If the data is not correct then decrease the value written to VGA_CONTROL_C(4:1) and repeat. The pixel location which is latched by VGA_DATA_BYTE_0, VGA_DATA_BYTE_1, and VGA_DATA_BYTE_2 is controlled by VIEW_PORT_DISPLAY_ORIGIN_LEFT_A(3:0). A new pixel is latched every line. To latch the first pixel after blank write ’0000’ to VIEW_PORT_DISPLAY_ORIGIN_LEFT_A(3:0). to latch the 16th pixel write ’1111’ to VIEW_PORT_DISPLAY_ORIGIN_LEFT_A(3:0).

If 16 bit or 24 bit color is used and the coloring is still incorrect then the clock/blank timing may not be correct. Write a different value to VGA_CONTROL_D(7:6) and repeat the above procedure.

To read the upper left hand corner of the VGA screen INTERRUPT_CONTROL and INTERRUPT_STATUS registers can be used.

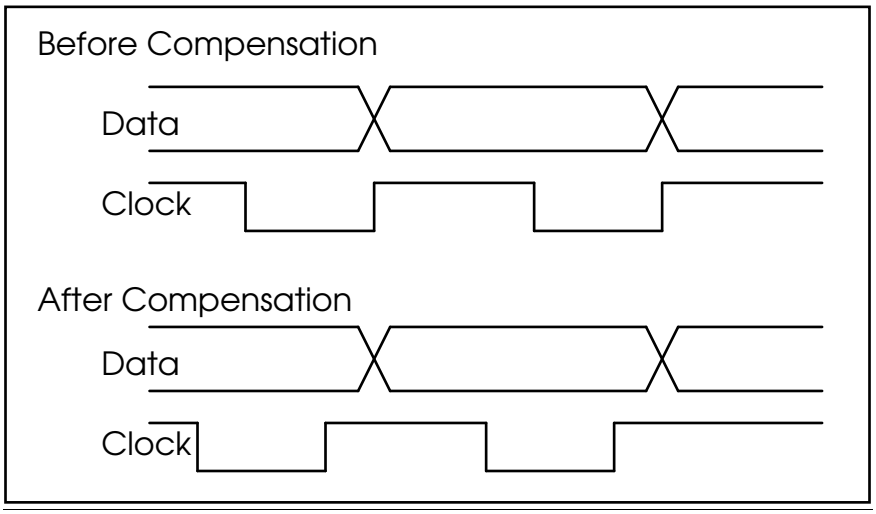


Figure 3.3.10 Clock Skewing

D2h, D3h Video Display Output Interrupt Control and Status Registers

VxP202 can be programmed to generate two display interrupts, VGA horizontal Sync. and VGA vertical Sync. There are two interrupt status bits, HSIS (bit 4, D3h) and VSIS (bit 5, D3h). These bits are set whenever a VGA vertical or horizontal interrupt is generated and are cleared when a read access is performed by the ISA bus. In addition, there are two real time SYNC status bits, VS (bit 1, D3h) and HS (bit 0, D3h). These bit represent the state of the horizontal and vertical Sync at the time that the status register is accessed.

A new bit was added in VxP202 rev B to the interrupt status register (bit 3) to provide software with observability of any underflowing situations with the videoout fifo. This bit is cleared on read. It is high if, at any time since the last read of this register, the videoout fifo has an underflow situation. Software can poll this register bit for several cycles after VxP202 operation has been set up, and make appropriate bandwidth concessions if this bit was at anytime high.

Important Note Regarding Clock Frequency for Videoout

Board setup and configuration must ensure that the internal video_clock frequency is 20MHz or higher if mem_clock frequency is 66MHz. If mem_clock frequency is 50MHz, then video_clock frequency must be 15MHz or higher. Note that the video_clock is divided down from vga_clock when :
- vga data input is high-color (16 bit) with double clock; vga_clock / 2 => video_clock
- vga data input is true-color (24 bit); vga_clock / 3 => video_clock
- in high-speed-bypass mode and one of the divide-down option is chosen (register 95H, bit 3-2)
- in hzoom-by-2 mode; vga_clock / 2 => video_clock

This low frequency limitation on video_clock is due to the complexity level of the read-counters of the async-fifo. A video_clock frequency lower than the values listed above may lead to lost data as the read pointer of the fifo doesn't keep up with the write pointer.

Determining VGA Mode

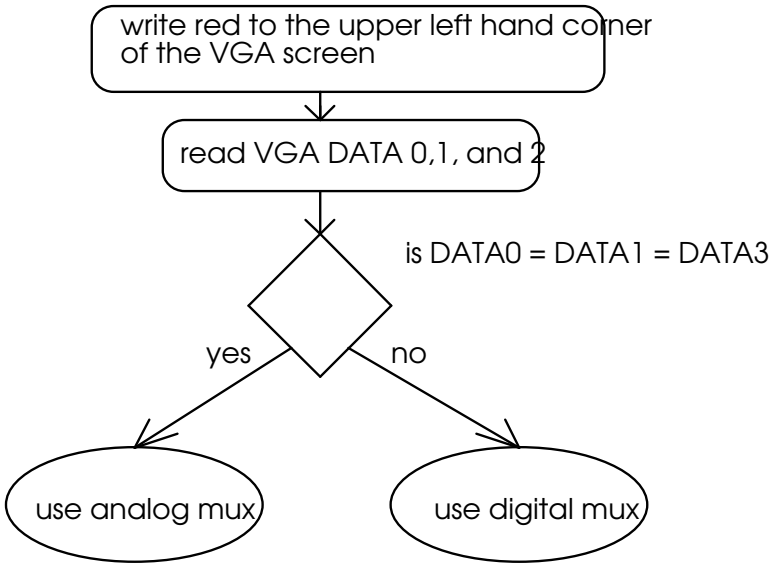
This section describes how to determine the mode which is best suited for the given VGA. The following items need to be known in order to provide the proper setup:

number of bits per pixel
number of clocks per pixel
RGB format
VGA clock frequency

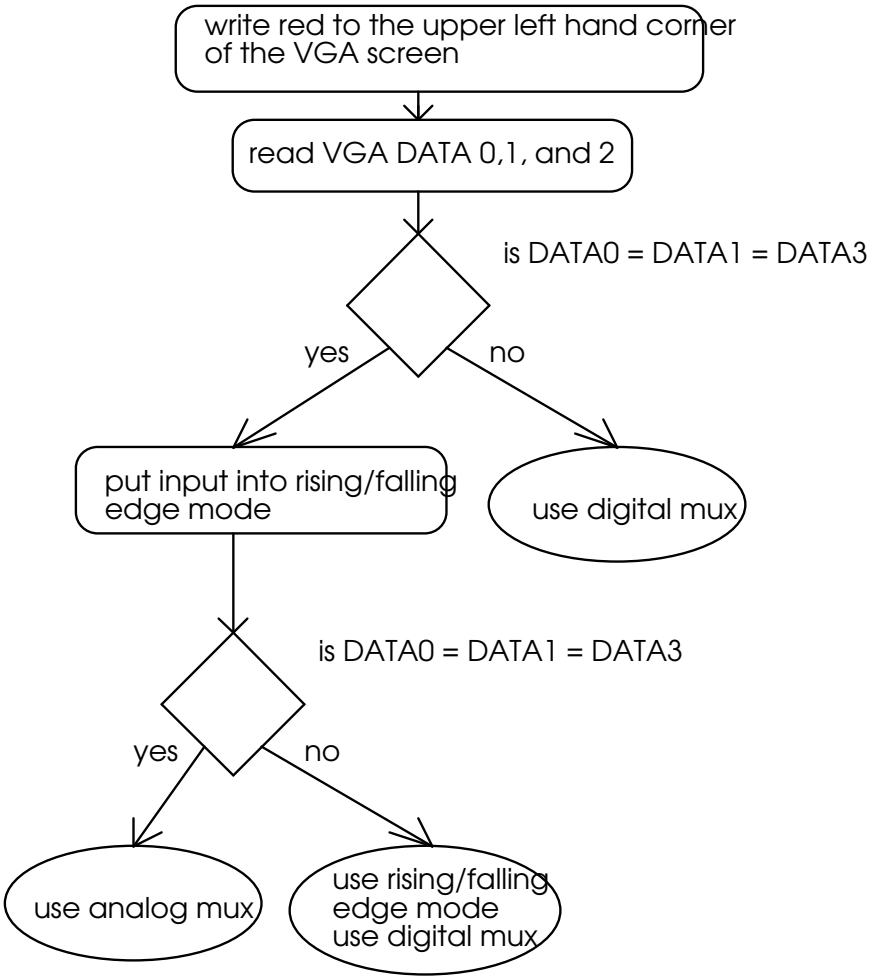
ASSUMPTIONS:
1) Software can determine the number of pixels per pixel (i.e. palettized, hi-color, true-color).
2) Software can determine wether hi-color RGB is 555 or 565.
3) Software can write to the upper left hand corner of the VGA screen.
4) Software can determine the clock speed of the VGA using frequency counter register.

In general digital muxing works better for hi-color and true-color VGAs. However, some VGAs output a divided clock so digital muxing is not possible. The flow diagrams shown below should be used to decide if the VGA clock has been divided. To read VGA data first write Eh into the least significant nibble of DISPLAY_WINDOW_LEFT_A (B0h) then read VGA_DATA_BYTE(0,1,2) (D5h - D7h).

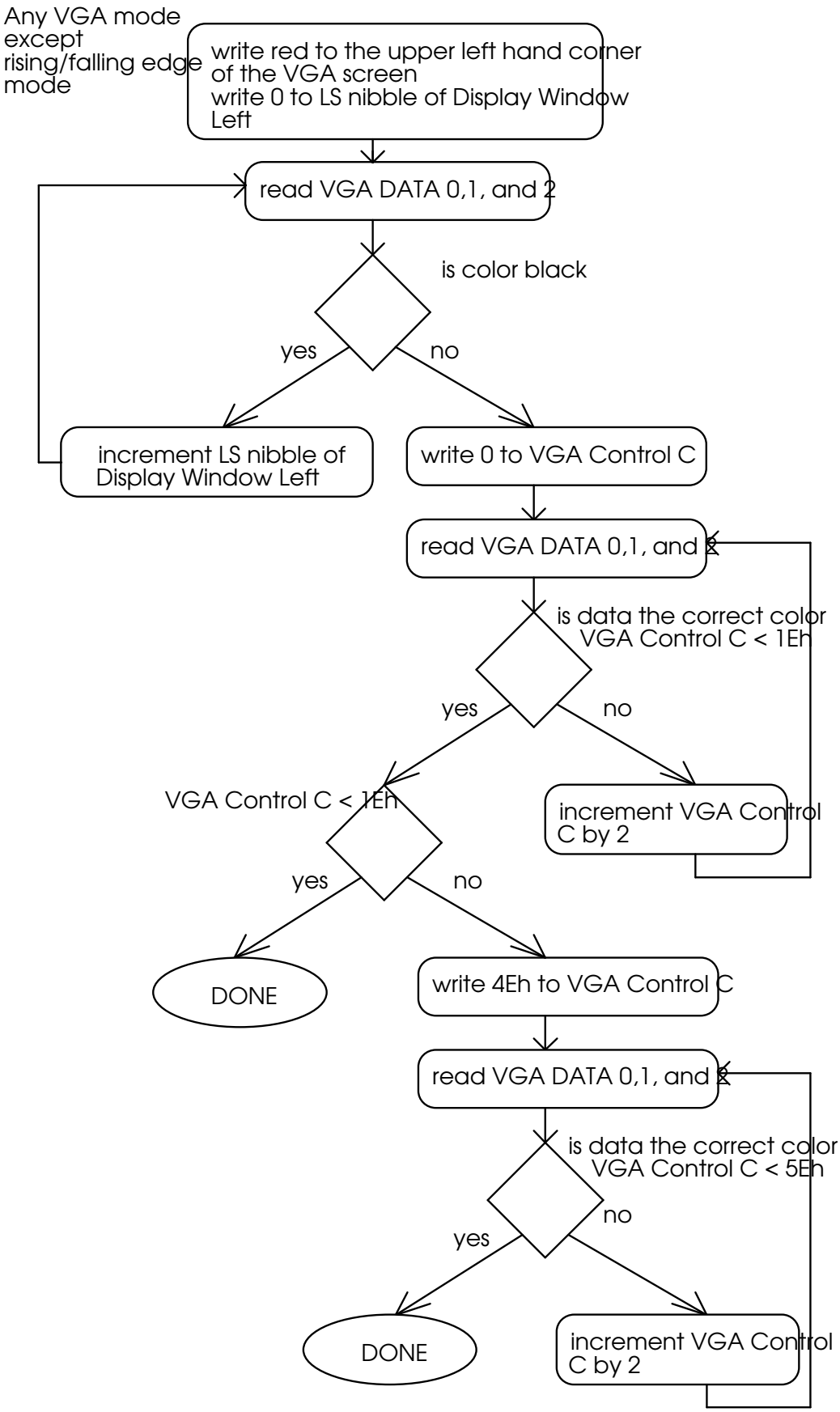
24 BIT COLOR

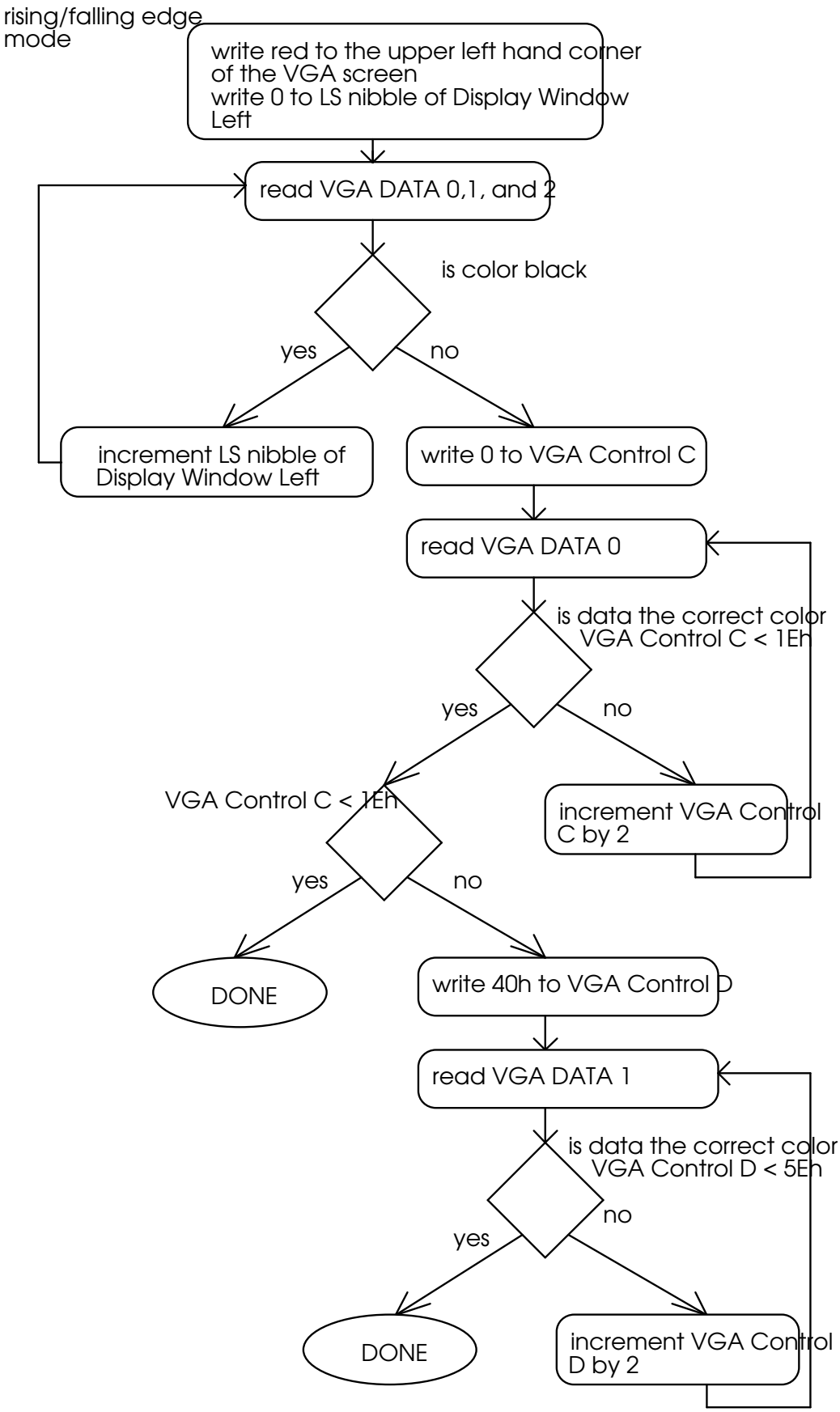


16 BIT COLOR



Determining VGA Clock Skew


Any VGA mode except rising/falling edge mode
write red to the upper left hand corner of the VGA screen
write 0 to LS nibble of Display Window Left
read VGA DATA 0,1, and 2
is color black
yes
no
increment LS nibble of Display Window Left
write 0 to VGA Control C
read VGA DATA 0,1, and 2
is data the correct color
VGA Control C < 1Eh
yes
no
VGA Control C < 1Eh
increment VGA Control C by 2
yes
no
DONE
write 4Eh to VGA Control C
read VGA DATA 0,1, and 2
is data the correct color
VGA Control C < 5Eh
no
yes
DONE
increment VGA Control C by 2


rising/falling edge mode
write red to the upper left hand corner of the VGA screen
write 0 to LS nibble of Display Window Left
read VGA DATA 0,1, and 2
is color black
yes
no
increment LS nibble of Display Window Left
write 0 to VGA Control C
read VGA DATA 0
is data the correct color
VGA Control C < 1Eh
yes
no
VGA Control C < 1Eh
increment VGA Control C by 2
yes
no
DONE
write 40h to VGA Control D
read VGA DATA 1
is data the correct color
VGA Control D < 5Eh
no
yes
DONE
increment VGA Control D by 2

3.4 Capture Register

The VxP202 allows the still-frame capture only due to band-width limitation. In case of 30 frames per second capture is required, please use VxP202 for your design.

Capture Pipeline Control & Status Registers

Index	Register Name
80h	Capture Control
84h - 85h	Capture View Port Width A & B
86h - 87h	Capture View Port Height A & B
88h	Capture Pixel Buffer Low & High Mark
8Ah	Capture Frame-Buffer (Multi-Buffer) Depth Control

To set up for capture, the above registers and the PX Bus Configuration (Index 12h) must be programmed. The Capture control holds 3 mode bits that configure and enable the capture pipeline. The View Port Width and Height registers define the memory window that the pipeline will read from and values written must be in terms of DRAM addressing. Index 88 holds 4 bits of both the low and high water marks. Since the capture FIFO is 32 deep, requiring 5 bit water marks, one bit of each mark is fixed and not writable. The MS Bit of the low water mark is fixed at "0" while the MS Bit of the high water mark is fixed at "1". The Multi-Biffer Depth Control register holds the pointer to the buffer release point. It points to 4-line groups. The Capture Pipeline will acquire a buffer and hold the Video Input pipeline out until it has read past the line group that the Depth Control register points to. The PX Bus Configuration register must be programmed to configure the type of capture. The modes that involve the Capture Pipeline are modes 00, 04, 02, 1A and 1B.

80h Capture Control Register

Bit	Default	R/W	Description
0	1	-	Reserved.
1	1	R/W	Capture Software Reset 0 - Capture Enabled 1 - Capture Disable (Capture Software Reset) This bit controls whether the capture pipeline is active or not. It is the software reset. When active high, the Capture Pipeline will be held in reset but related register will not be effected. This bit must be 0 to program any registers pertaining to the capture pipeline since the registers are not synchronized to the capture pipeline.
2	1	-	Reserved.

Capture View Port Address Height and Width Registers

VxP202's capture view port's size can be independent from the acquisition and display window. The capture start address is fixed and points to the upper left hand corner of the buffer window in the video frame buffer. The width and height specify the window size in terms of DRAM viewport addressing. If software wants to capture the same video data that is being acquired, the width and height of the capture window should be the same as the final video input size (cropped and scaled). Three values must be determined in order to perform a capture. These are the values stored in the width and height registers, and the number of software read accesses required.

The acquisition viewport width is based upon two mode settings, namely the memory mode (ISA Control, index 30h), the video layout (Video Layout Control, index 73h) and the interleave factor (number of pixels per DRAM location). The memory mode bit sets the width of the DRAM data path (8 or 16 bits). The video layout bits set the video buffer partitioning (the four multi-buffer modes). The outline below shows how memory is partitioned based upon the video layout and memory mode settings:

video_layout = 0
- mem_mode = 0 (8-bit)
  - width = 512 blocks (512 bytes), height = 512 lines, buffers = 1
- mem_mode = 1 (16-bit)
  - width = 512 blocks (1024 bytes), height = 512 lines, buffers = 1

video_layout = 1
- mem_mode = 0 (8-bit)
  - width = 512 blocks (512 bytes), height = 256 lines, buffers = 2
- mem_mode = 1 (16-bit)
  - width = 256 blocks (512 bytes), height = 512 lines, buffers = 2

video_layout = 2
- mem_mode = 0 (8-bit)
  - width =256 blocks (256 bytes), height = 1024 lines, buffers = 1
- mem_mode = 1 (16-bit)
  - width = 256 blocks (512 bytes), height = 1024 lines, buffers = 1

video_layout = 3
- mem_mode = 0 (8-bit)
  - width = 256 blocks (256 bytes), height = 256 lines, buffers = 4
- mem_mode = 1 (16-bit)
  - width = 256 blocks (512 bytes), height = 256 lines, buffers = 4

The above block width value shows the maximum width that the viewport can span. If it is set beyond this value, the capture read pointer will back wrap around to the begining of the line as it reads every line. The formula below shows how to determine the width of the viewport in memory.

Viewport Width = (pixel width) * (video input horizontal scale factor) / (# pixels per DRAM location)

The "pixel width" is the incoming video width after cropping and before scaling. The "# pixels per DRAM location" is the interleave factor. With 422, it is 2 for a 16-bit memory mode and 1 for an 8-bit memory mode. With 411, it is 8/3 for a 16-bit memory mode and 4/3 for an 8-bit memory mode. If there is a remainder after calculating the width, round to the next highest integer.

The viewport height can be up to the "height" value shown in the above outline. If it is set beyond this maximum, the capture read pointer will wrap back around to the begining of the buffer. If incoming video is being acquired from an NTSC decoder, it will be in an interlaced format at the interface to the input pipeline. Only one field is written to a buffer at a time, and lines are written in succession. In other words, a line will not be skipped between lines of a given field. The viewport height is simply the field height times the video input vertical scale factor (5Bh,5Ch).

Software Capture -- Avoiding Timeouts

When doing software capture directly from VxP202, it is important to perform a read access only when data is available in the capture pipeline. If it is not, the read will be held up as the VxP202 inserts wait states. The cycle may eventually be aborted when the "timeout counter" reaches zero. This timeout counter is always initiated at the begining of a read or write, memory or IO command and is allowed to count down. If a read cycle is long and the counter reaches zero, the cycle will be terminated and invalid data will be read. If the next read cycle is not terminated, valid data will be read and the capture stream will continue as it would normally. Whenever a cycle is terminated in this manner, the ISA timeout interrupt pending regsiter is set (ISA Control, Index 30h). If unmasked, this bit will also generate an interrupt.

The capture pipeline can be monitored for data by polling the capture FIFO bit of the Interrupt Status Register (Index 61h) or by enabling that bit to cause an interrupt. Interrupts are enabled in the Interrupt Control Register (Index 60h). When pipeline full event occurs, this pending bit is set and it remains set until software clears it. This means that the bit must be cleared before the event is given a chance to occur. In other words, clear this bit before capture is started (before the capture software reset is cleared, 80h). After capture is started wait for the capture FIFO bit to be set. When the bit is detected active, clear it, perform the block read with the correct number of reads, then wait for the capture FIFO bit to be set again before clearing it again and performing the next block read.

The number of 16-bit read accesses that software must make, depends on the memory data type setting (Input Configuration B, 39h), the capture decoder enable (Capture Control, 80h), the capture viewport width and height settings, the memory mode setting (ISA Control, index 30h), and the interleave factor (Video Layout Control, index 73h, and memory mode setting).

When the capture decoder is enabled:

- When the memory data type is set to 411
  - # Horiz. Groups = Round Down [(cap. viewport width) / 3]
  - Left-over = (cap. viewport width) mod 3
  - When mem_mode = 0 (8-bit DRAM data bus)
    - When Left-over =
      - 0 -- Horiz. Count = (4 * # Horiz. Groups)
      - 1 -- Horiz. Count = (4 * # Horiz. Groups) + 1
      - 2 -- Horiz. Count = (4 * # Horiz. Groups) + 2
  - When mem_mode = 1 (16-bit DRAM data bus)
    - When Left-over =
      - 0 -- Horiz. Count = (8 * # Horiz. Groups)
      - 1 -- Horiz. Count = (8 * # Horiz. Groups) + 2
      - 2 -- Horiz. Count = (8 * # Horiz. Groups) + 5
- When the memory data type is set to 422
  - When mem_mode = 0 (8-bit DRAM data bus)
    - Horiz. Count = (cap. viewport width)
  - When mem_mode = 1 (16-bit DRAM data bus)
    - Horiz. Count = 2*(cap. viewport width)

Reads = (Horiz. Count) * (cap. viewport height)

When the capture decoder is disabled:

- When mem_mode = 0 (8-bit DRAM data bus)
  - # Reads = (cap. viewport width) * (cap. viewport height) / 2
- When mem_mode = 1 (16-bit DRAM data bus)
  - # Reads = (cap. viewport width) * (cap. viewport height)

The "Round Down" function above implies rounding down to the next integer when a remainder results. When the capture decoder is enabled, compressed data read from DRAM is decompressed and converted to a 16-bit YUV 422 format (even if the memory data type is 411). Each word read will provide a 16-bit YU or YV pixel. The low byte will always hold Y. The high byte will hold U on even reads and V on odd reads. The "Horiz. Count" calculated above represents the number of pixels (Y-values), after decompression, that each line holds.

If the decoder is disabled, data is passed through without modification. It will be in a differentially compressed format that will depend on the memory data type setting. The following tables describe the formats for differentially compressed YUV data:

Differential YUV411

READ COUNT MOD 3 = 0

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
V3	V2	V1	V0	Y3	Y2	Y1	Y0	U3	U2	U1	U0	Y3	Y2	Y1	Y0

READ COUNT MOD 3 = 1

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
U3	U2	U1	U0	Y3	Y2	Y1	Y0	Y3	Y2	Y1	Y0	Y3	Y2	Y1	Y0

READ COUNT MOD 3 = 2

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Y3	Y2	Y1	Y0	Y3	Y2	Y1	Y0	V3	V2	V1	V0	Y3	Y2	Y1	Y0

Differential YUV422

EVEN WORDS

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
V3	V2	V1	V0	Y3	Y2	Y1	Y0	U3	U2	U1	U0	Y3	Y2	Y1	Y0

ODD WORDS (SAME AS EVEN)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
V3	V2	V1	V0	Y3	Y2	Y1	Y0	U3	U2	U1	U0	Y3	Y2	Y1	Y0

If the capture decoder is disabled (capturing compressed YUV data), there may be partially filled data words at the end of each line. For the compressed YUV411 format, to find where the valid data ends in the last word read of each line, use the following chart:

X = { (YUV422 line width at input to front end) * (horiz. scale factor) } mod 8

X	Used Data	16-bit Mem. Mode, Word Read mod 3	8-bit Mem. Mode, Word Read mod 3
0	YU	0	0
1	YV	0	1
2	Y	1	2
3	Y	1	2
4	YU	1	0
5	YV	2	1
6	Y	2	2
7	Y	2	2